

LCFC Confidential

BMWC1&C2 M/B Schematics Document NM-A471 REV:0.4

Intel Braswell M-Processor with DDRIIIL + NV (N16V-GM) GPU

2015-03-23

REV:0.4

Security Classification		LC Future Center Secret Data		Title					
Issued Date		2014/09/24		Deciphered Date				2015/03/23	
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						Custom	BMWC1		0.4
						Date:			Tuesday, April 07, 2015

Power Plane State	B+ +3VL	+3VALW +5VALW	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_FCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	EC +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

EC SM Bus2 address

PCH SM Bus address

Device	Device	Address
Smart Battery	0001 011X b	1001_100xb(reserve)
Charger	need to update	0x9E(base on NV default)
	Thermal Sensor EMC1403-2	
	VGA	

Device	Address
DDR DIMMA	1010 000Xb
Wlan	Rsvd
TP	need to update

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 3.0 Ports		
XHCI	Port	Port device
USB 3.0	0	USB Port (Left Side)
	1	USB3.0 Card Reader
USB 2.0	0	USB Port (Left Side)
	1	USB Port (Right Side)
	2	BT
	3	Camera
	4	USB Port (Right Side)
USB HUB	1	
	2	
	3	
	4	

PCIE PORT LIST

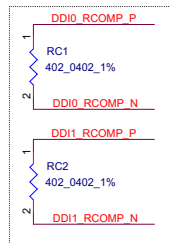
Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

BOM Structure Table

[illegible]

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI



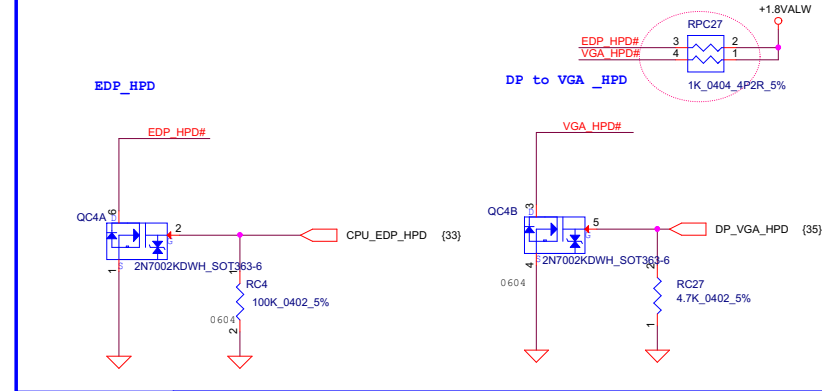
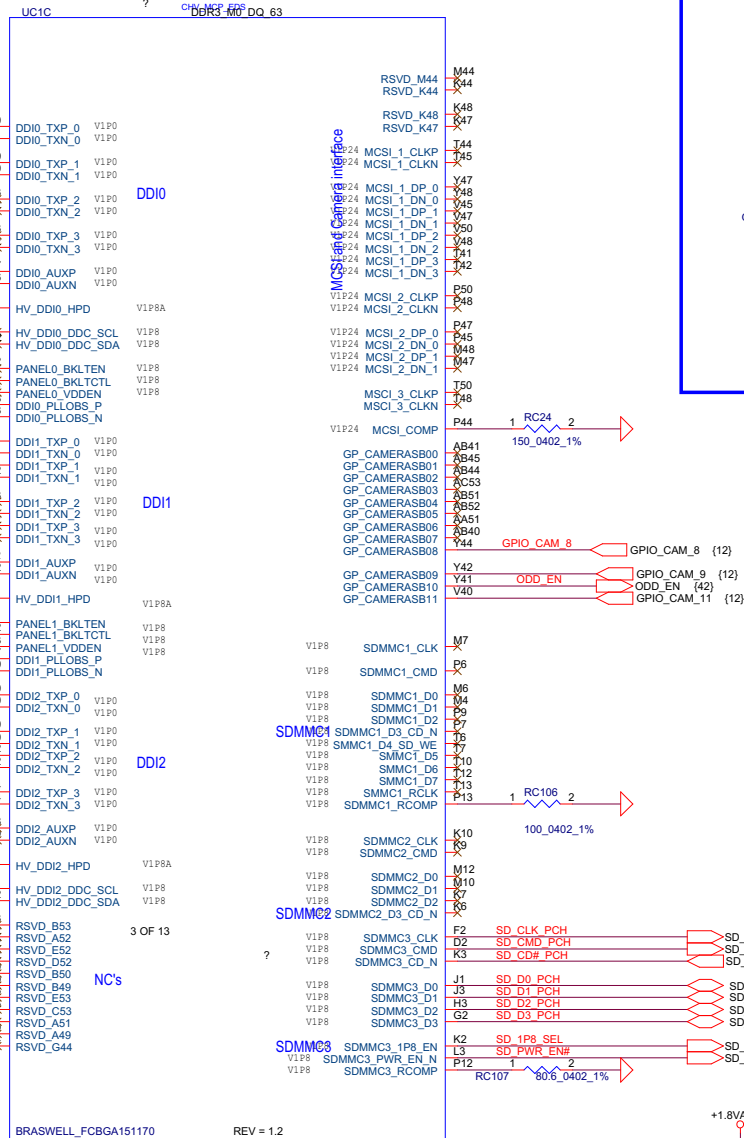
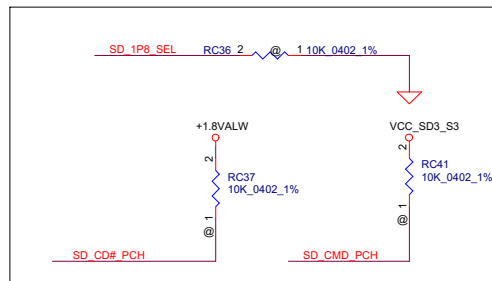
DP TO VGA Converter

EDP

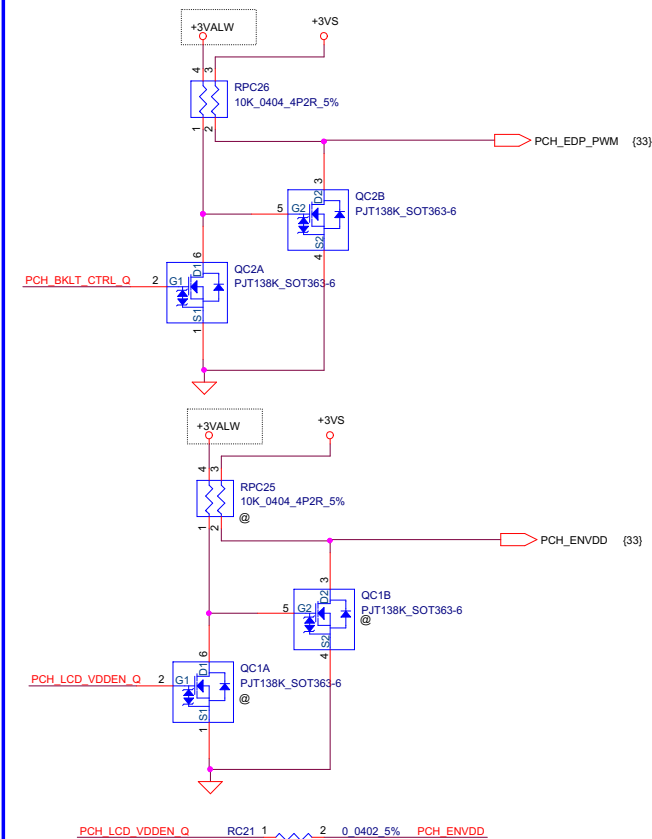
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

DDI PORT LIST

Port	Device
DDI0	DP TO VGA
DDI1	eDP
DDI2	HDMI

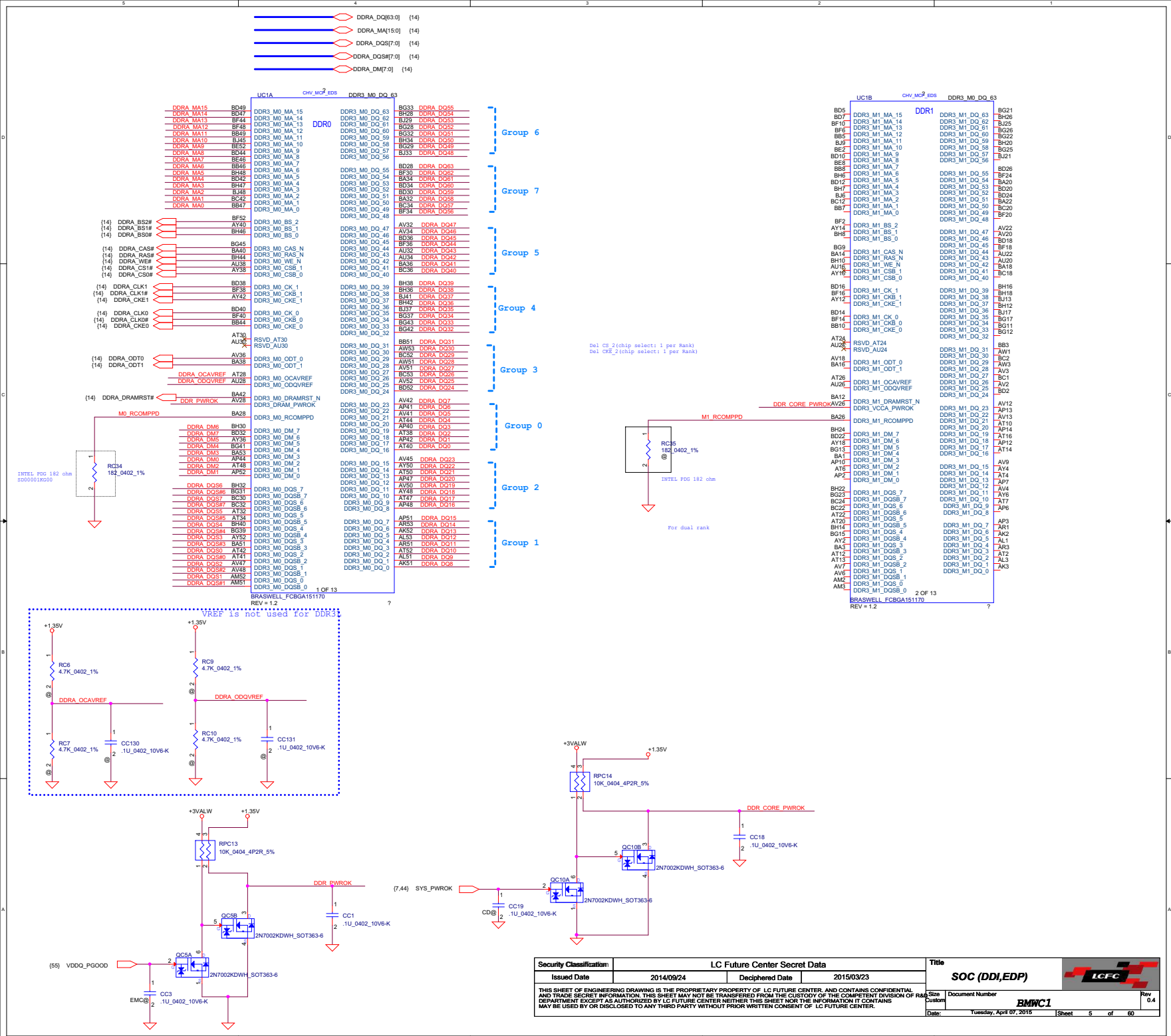


PCH_ENBKL can direct connect to EC for costdown



PCH_LCD_VDDEN_Q VOH min is 1.8-0.45=1.35V, need level shift

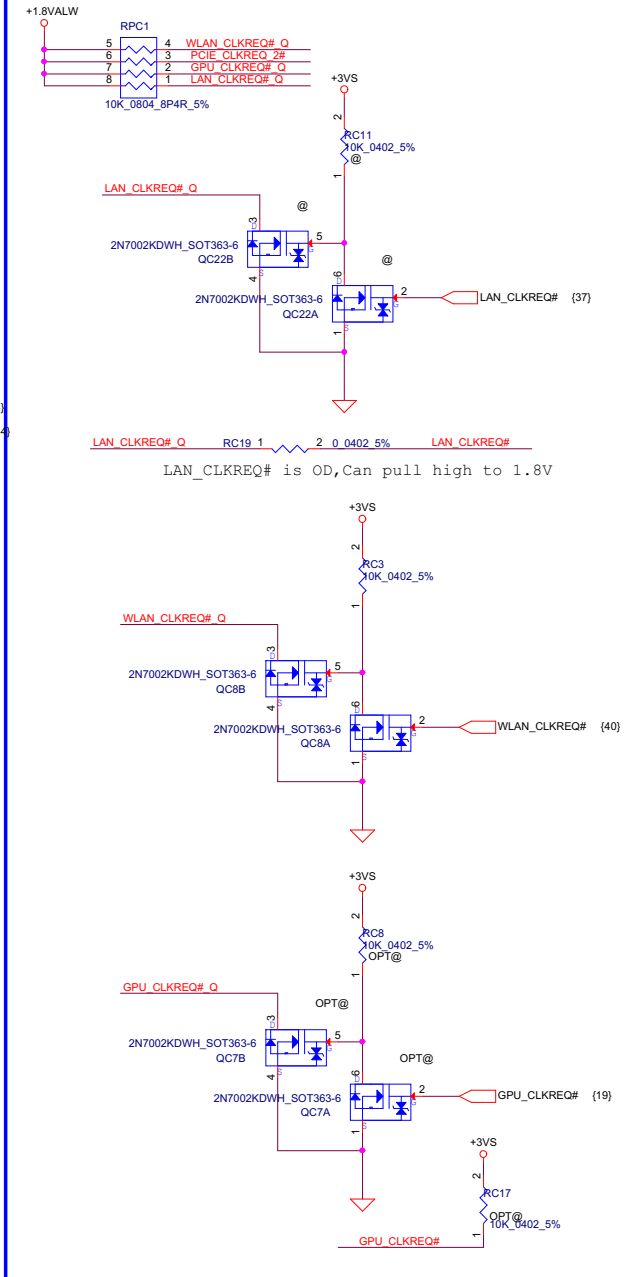
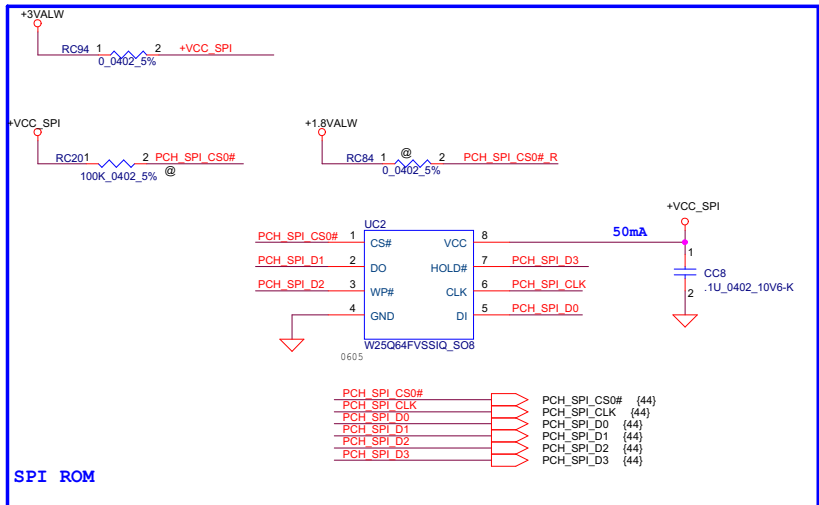
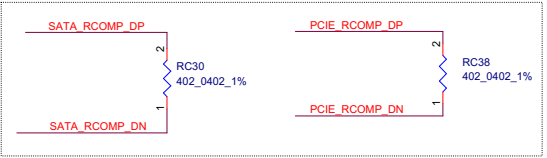
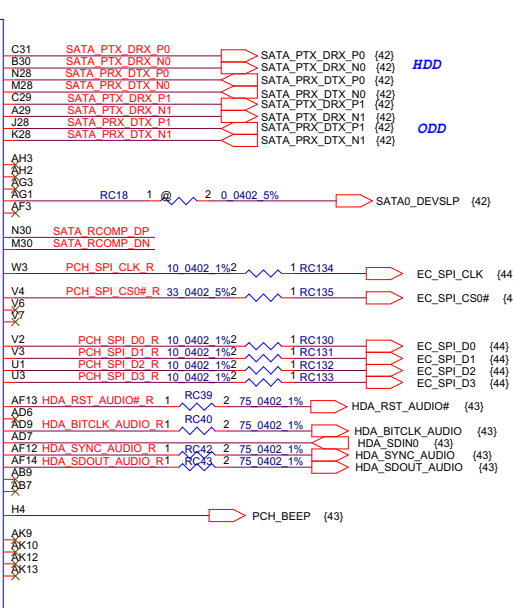
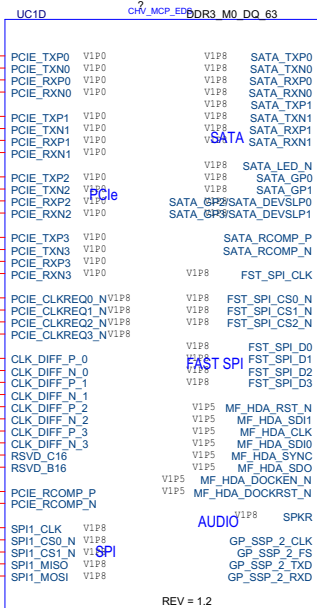
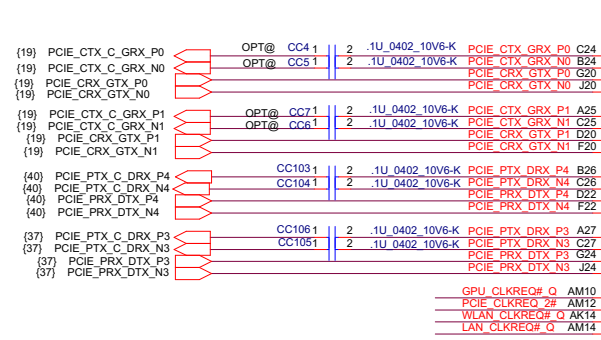
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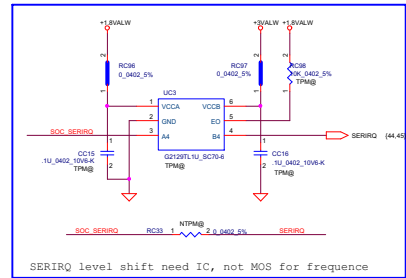
dGPU

WLAN

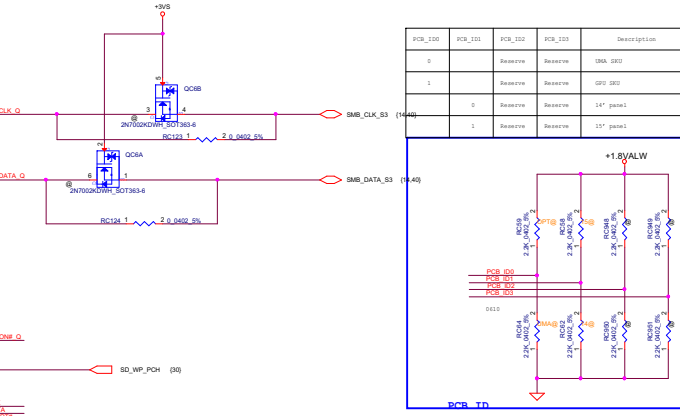
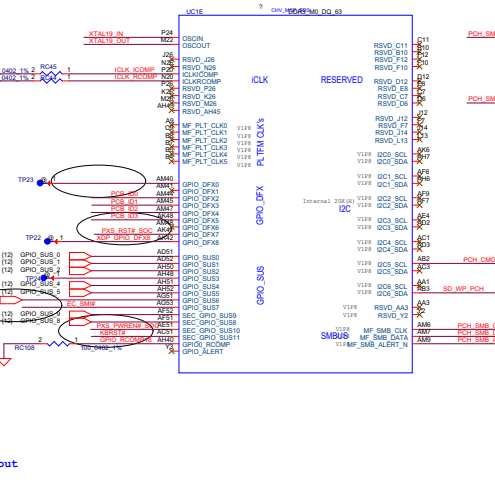
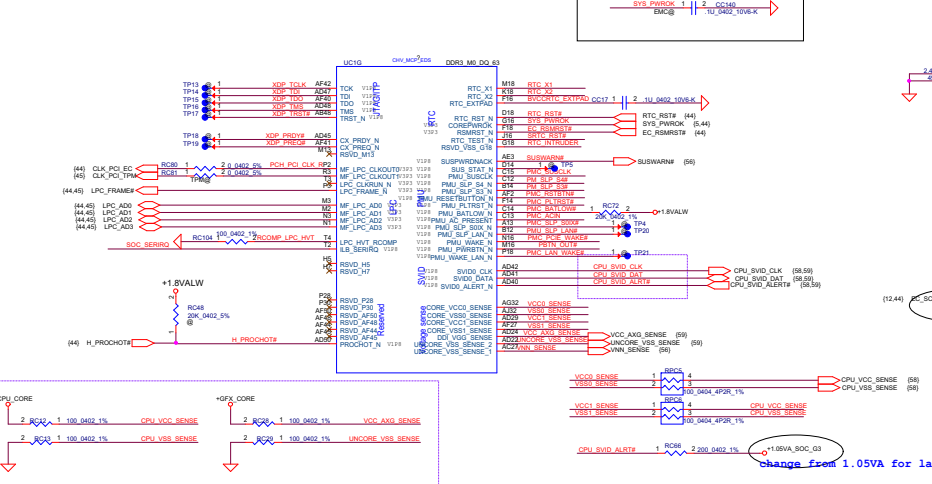
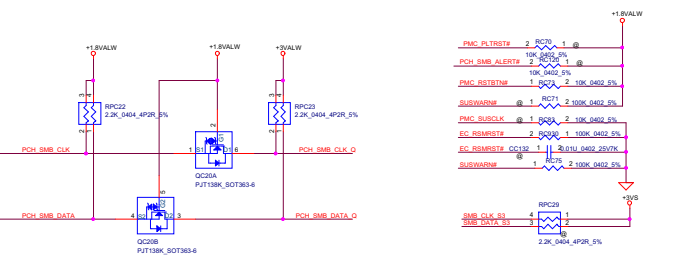
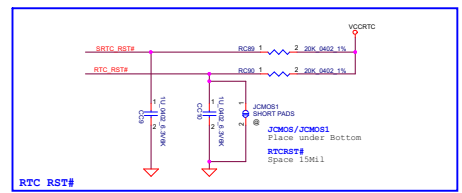
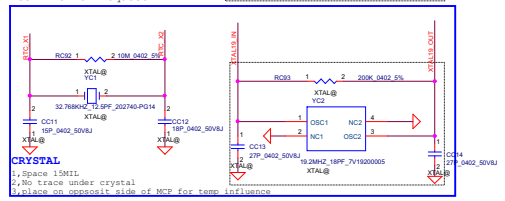
LAN



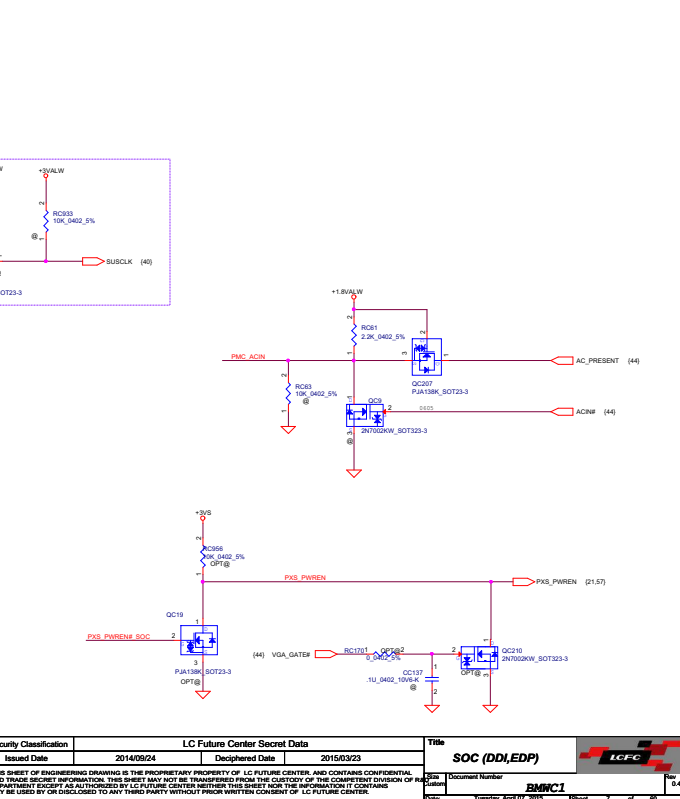
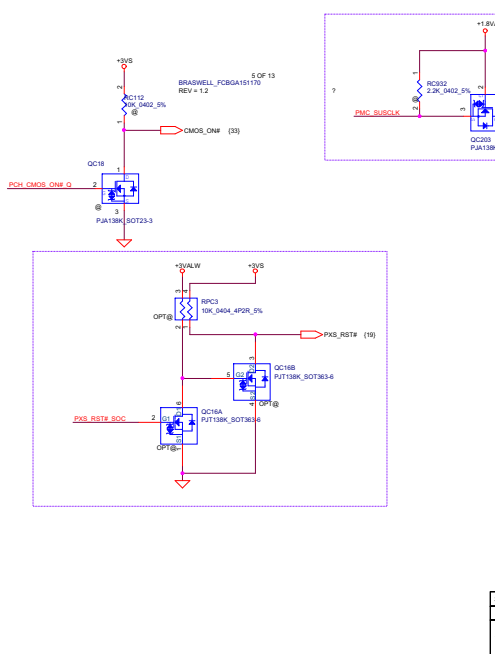
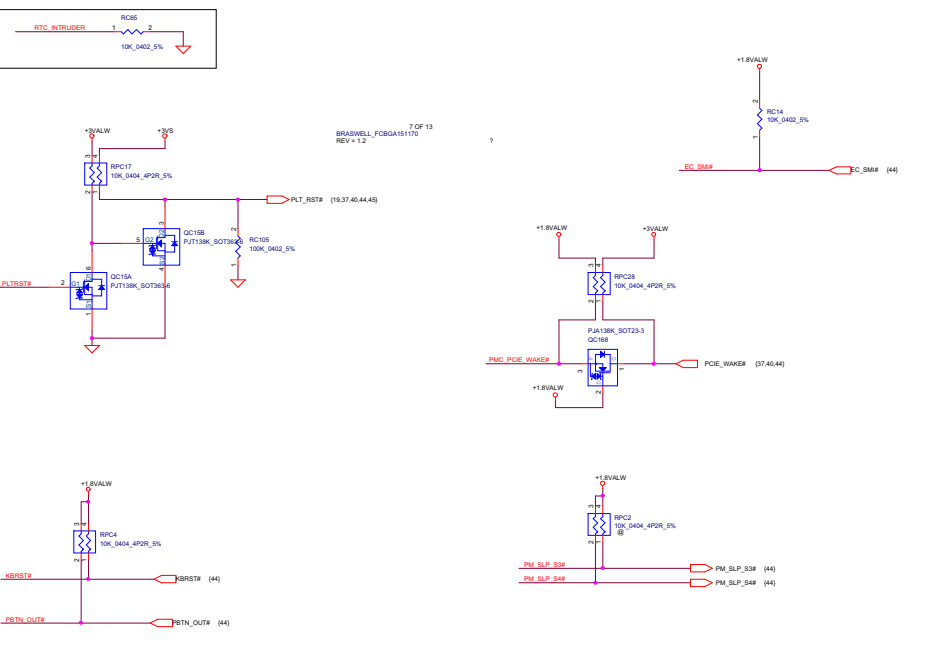
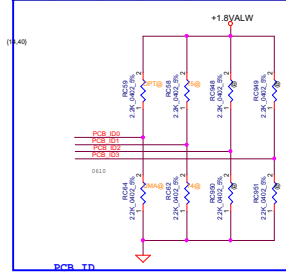
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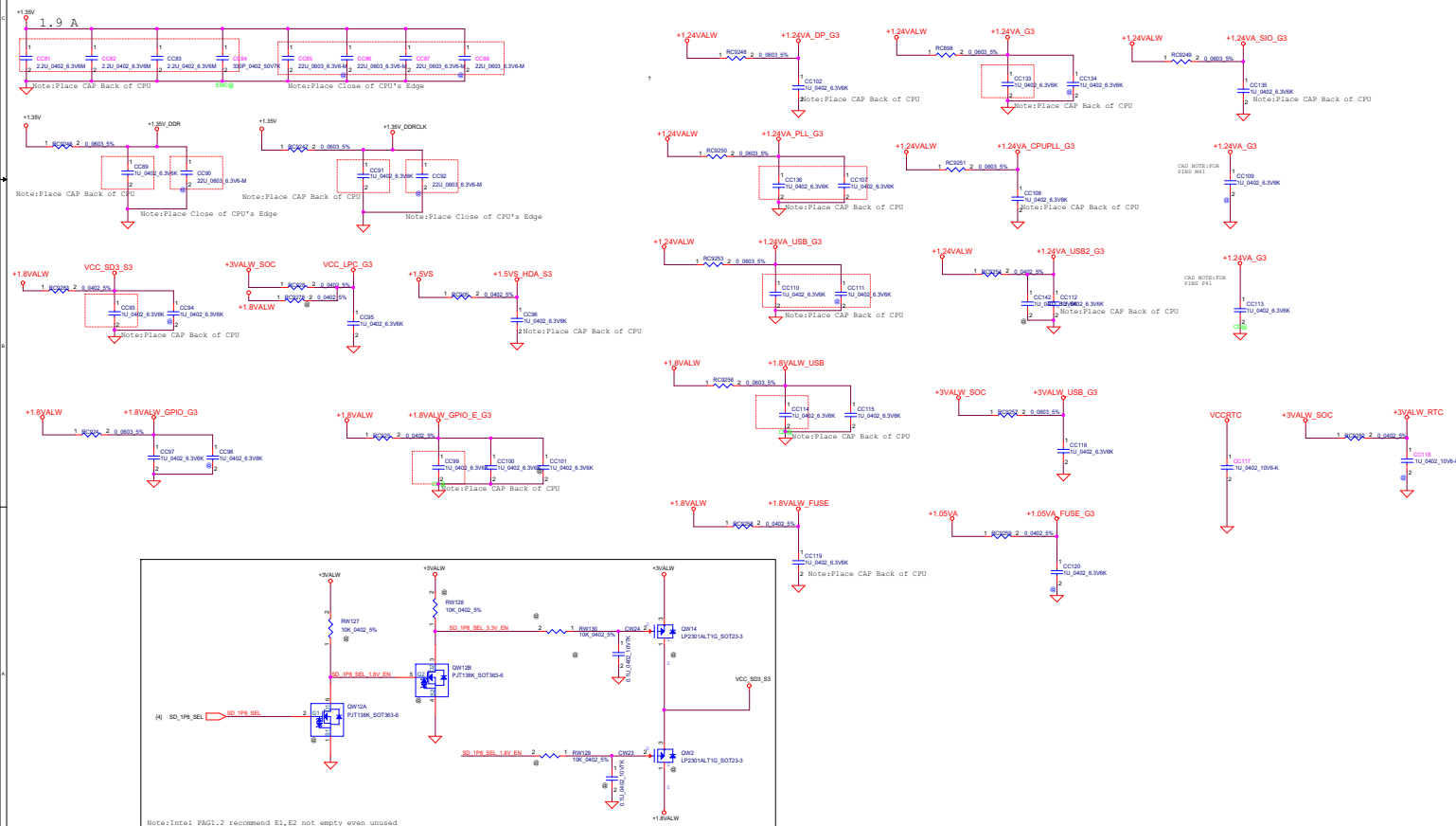
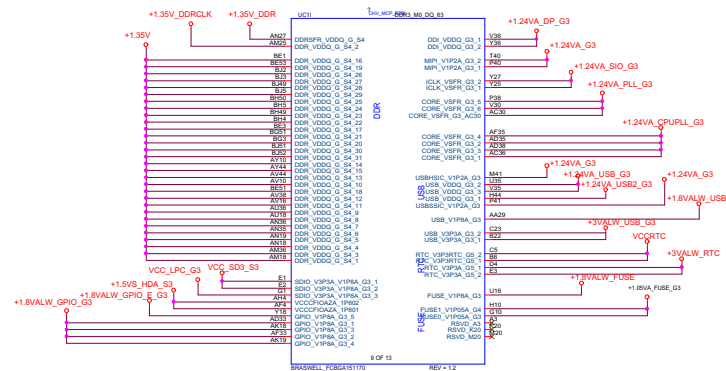


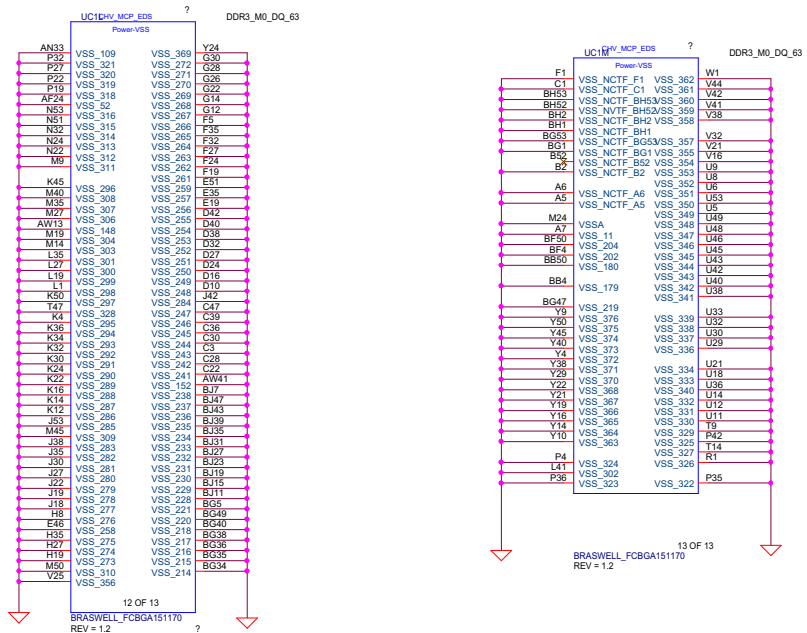
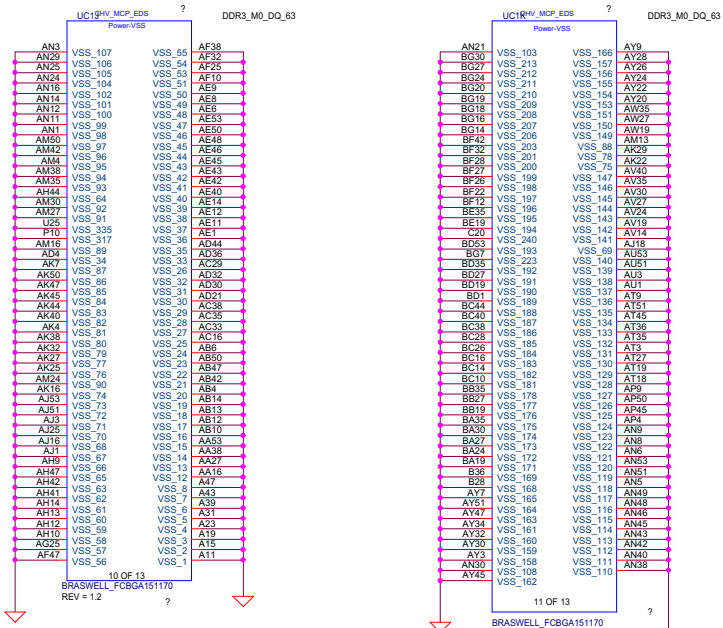
32.768K need change to SJ10000IM00,
as intel EDS New request



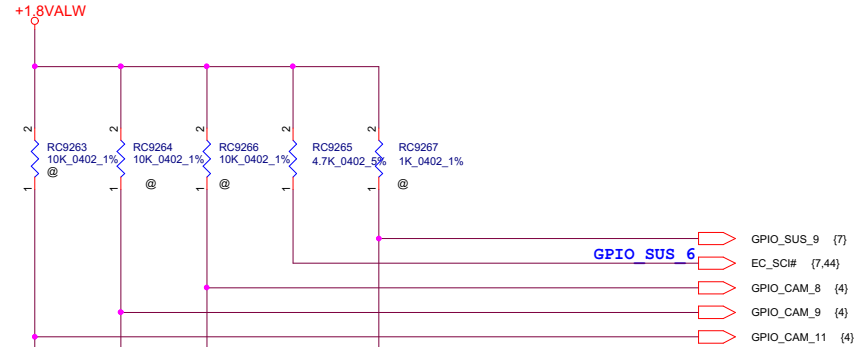
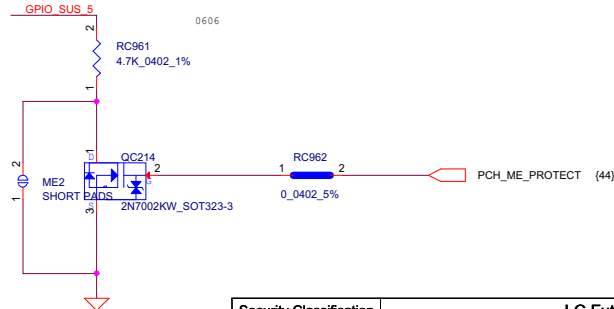
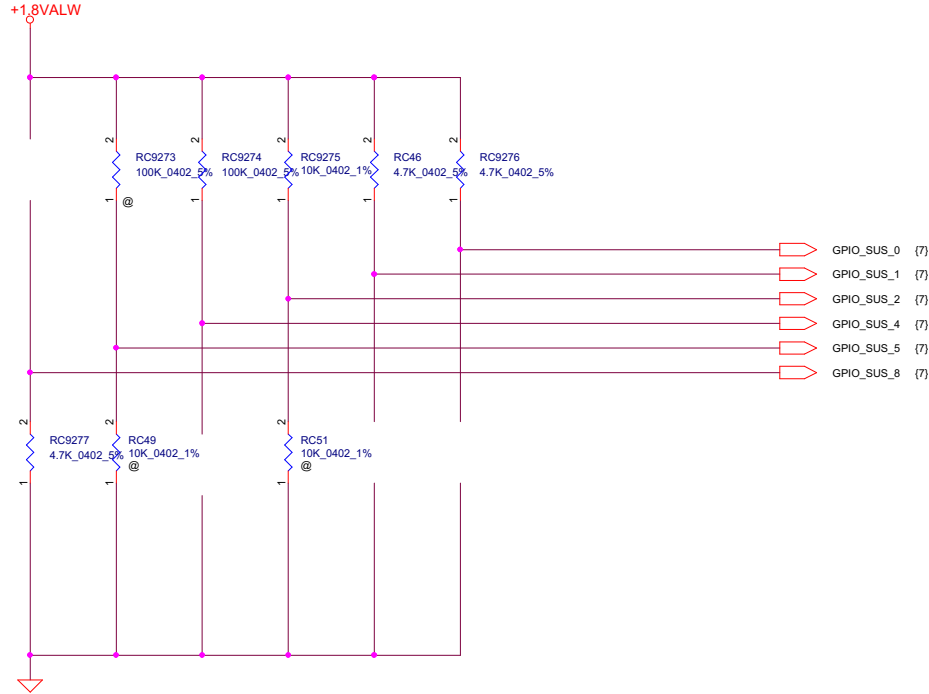
PCB_100	PCB_101	PCB_102	PCB_103	Description
0	Reserved	Reserved	Reserved	Reserved
1	Reserved	Reserved	Reserved	Reserved
2	Reserved	Reserved	Reserved	Reserved
3	Reserved	Reserved	Reserved	Reserved



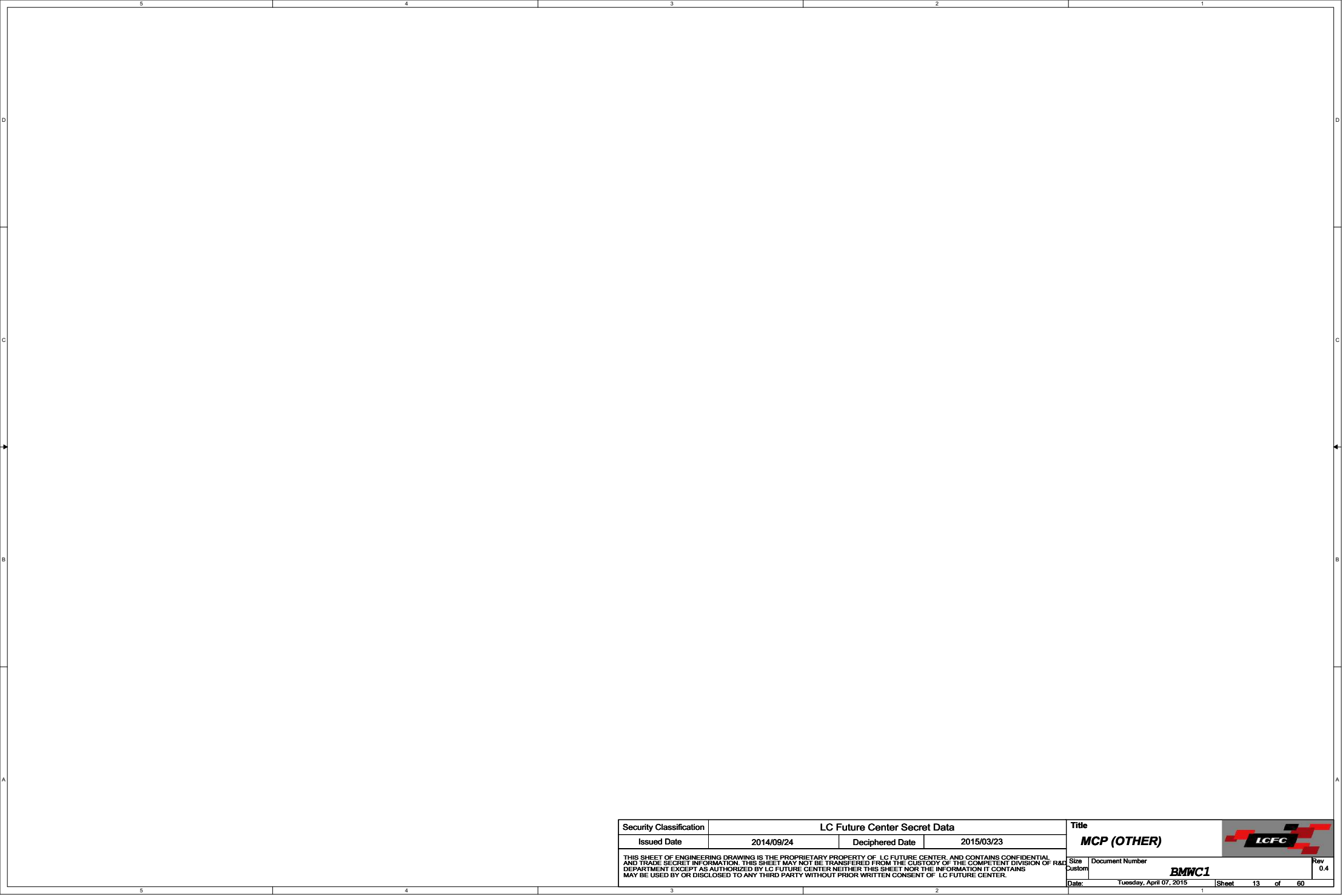




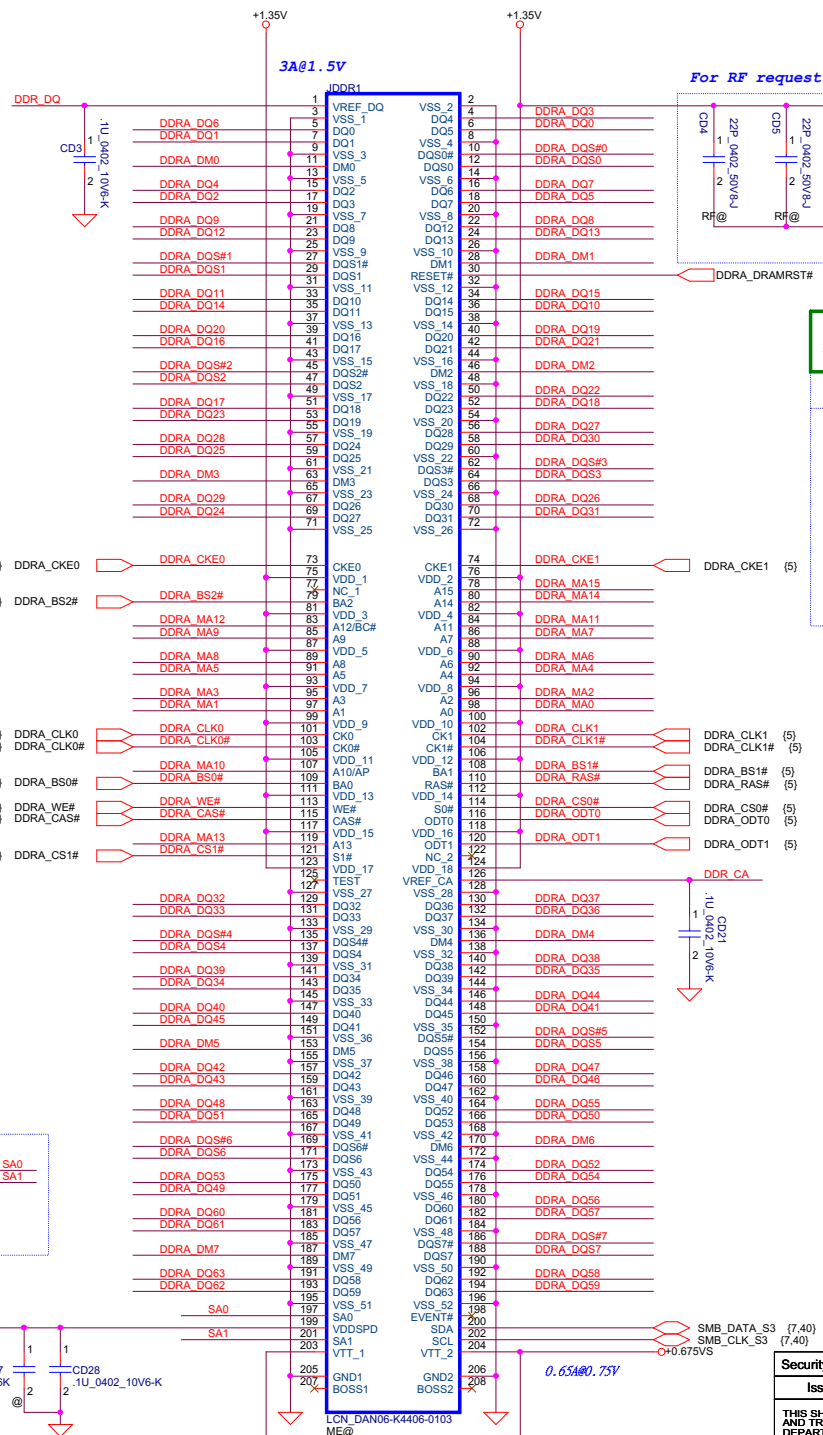
Hardware STRAPS (Follow up CRB)



Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected Note: DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the p/n floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation Note: This strap MUST be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass



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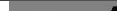
DDR3 SO-DIMM A $2.2U_{\text{L}}$ 

The diagram shows a circuit with a +0.675V source connected to a network of capacitors and inductors. The components are labeled as follows:

- CD24: 1U 0402 5.30E-6
- CD23: 1U 0402 5.30E-6
- CD25: .1U 0402 10V-6K
- CD26: .1U 0402 10V-6K
- CD27: 10U 0803 6.96M
- CD28: 10U 0803 6.96M
- CD29: 22P 0402 50V-8-4

Annotations on the diagram include:

- A red box around CD23 and CD24 with the text: "cost down bom to change 0.1uF".
- A red arrow pointing to CD26 with the text: "For RF request".

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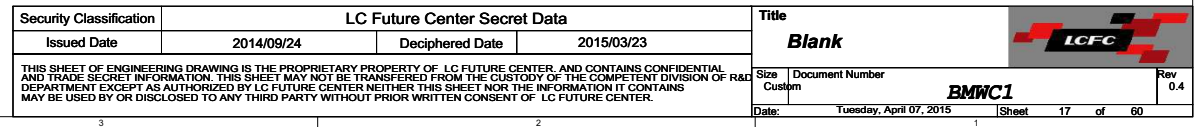
Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDRBDQ17
7	DQ1	DDRBDQ23
15	DQ2	DDRBDQ18
17	DQ3	DDRBDQ21
4	DQ4	DDRBDQ16
6	DQ5	DDRBDQ22
16	DQ6	DDRBDQ19
18	DQ7	DDRBDQ20
10	DQS#0	DDRBDQS#2
12	DQS0	DDRBDQS2
21	DQ8	DDRBDQ3
23	DQ9	DDRBDQ5
33	DQ10	DDRBDQ6
35	DQ11	DDRBDQ1
22	DQ12	DDRBDQ2
24	DQ13	DDRBDQ4
34	DQ14	DDRBDQ0
36	DQ15	DDRBDQ7
27	DQS#1	DDRBDQS#0
29	DQS1	DDRBDQS0
39	DQ16	DDRBDQ8
41	DQ17	DDRBDQ10
51	DQ18	DDRBDQ14
53	DQ19	DDRBDQ15
40	DQ20	DDRBDQ13
42	DQ21	DDRBDQ12
50	DQ22	DDRBDQ9
52	DQ23	DDRBDQ11
45	DQS#2	DDRBDQS#1
47	DQS2	DDRBDQS1
57	DQ24	DDRBDQ27
59	DQ25	DDRBDQ26
67	DQ26	DDRBDQ28
69	DQ27	DDRBDQ24
56	DQ28	DDRBDQ31
58	DQ29	DDRBDQ30
68	DQ30	DDRBDQ29
70	DQ31	DDRBDQ25
62	DQS#3	DDRBDQS#3
64	DQS3	DDRBDQS3
129	DQ32	DDRBDQ33
131	DQ33	DDRBDQ36
141	DQ34	DDRBDQ39
143	DQ35	DDRBDQ38
130	DQ36	DDRBDQ37
132	DQ37	DDRBDQ32
140	DQ38	DDRBDQ35
142	DQ39	DDRBDQ34
135	DQS#4	DDRBDQS#4
137	DQS4	DDRBDQS4
147	DQ40	DDRBDQ40
149	DQ41	DDRBDQ43
157	DQ42	DDRBDQ42
159	DQ43	DDRBDQ44
146	DQ44	DDRBDQ45
148	DQ45	DDRBDQ41
158	DQ46	DDRBDQ46
160	DQ47	DDRBDQ47
152	DQS#5	DDRBDQS#5
154	DQS5	DDRBDQS5
163	DQ48	DDRBDQ52
165	DQ49	DDRBDQ51
175	DQ50	DDRBDQ50
177	DQ51	DDRBDQ48
164	DQ52	DDRBDQ49
166	DQ53	DDRBDQ53
174	DQ54	DDRBDQ54
176	DQ55	DDRBDQ55
169	DQS#6	DDRBDQS#6
171	DQS6	DDRBDQS6
181	DQ56	DDRBDQ62
183	DQ57	DDRBDQ57
191	DQ58	DDRBDQ59
193	DQ59	DDRBDQ63
180	DQ60	DDRBDQ56
182	DQ61	DDRBDQ61
192	DQ62	DDRBDQ58
194	DQ63	DDRBDQ60
186	DQS#7	DDRBDQS#7
188	DQS7	DDRBDQS7

0.65400.75V

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5		4		3		2		1	
D									
C									
B									
A									



N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

	GPU (4)	Mem (1.5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V)		I/O and PLL VDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

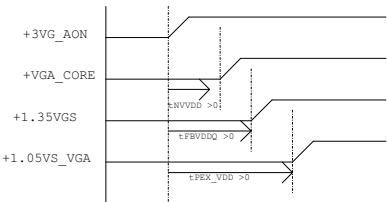
N15x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

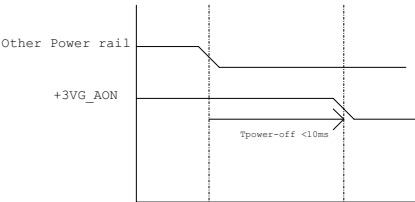
SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence

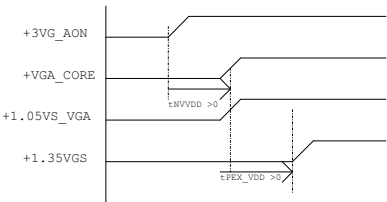


1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimum system VDD33 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence



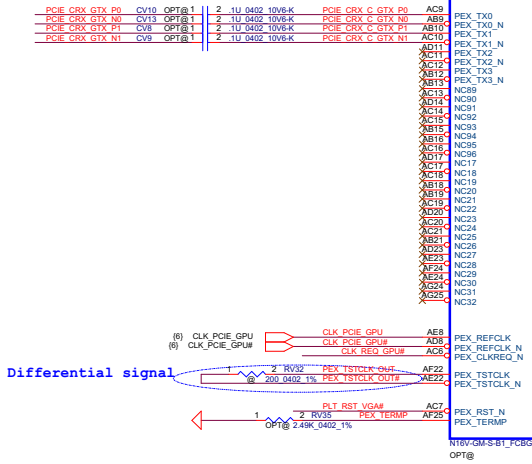
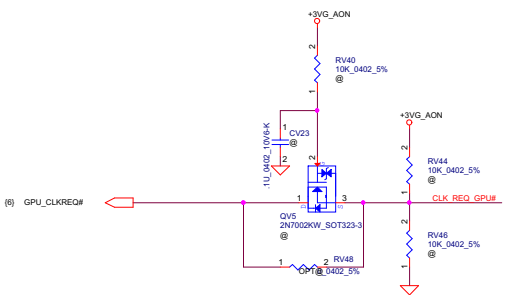
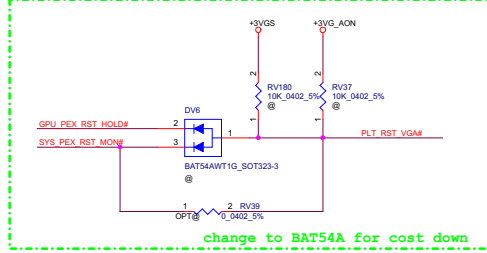
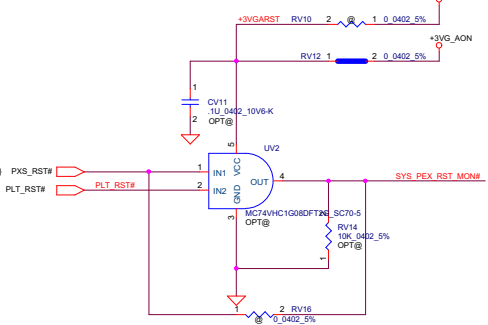
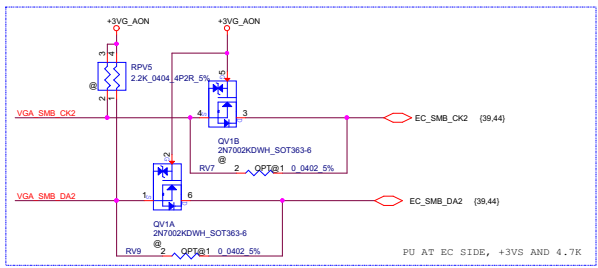
1. all power rail ramp up time should be larger than 40us

N15x Binary Straps

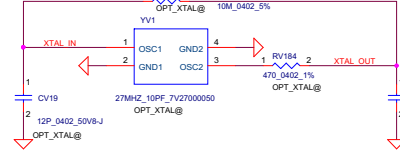
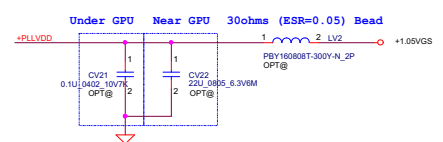
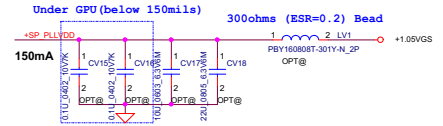
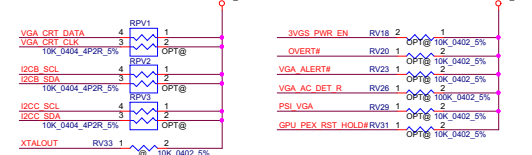
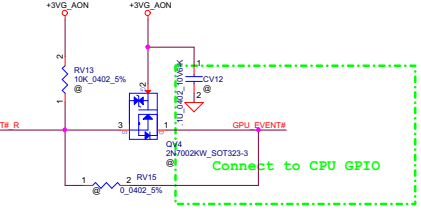
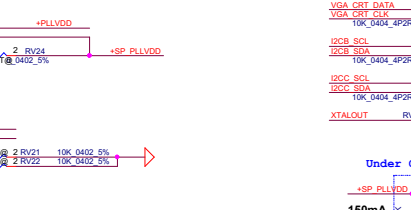
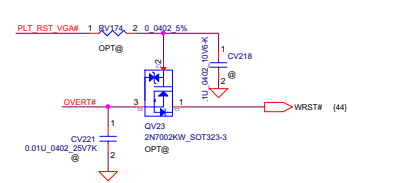
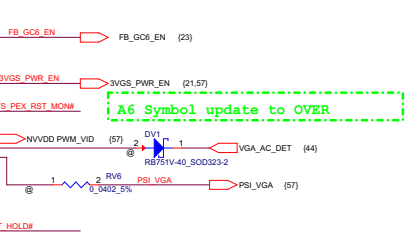
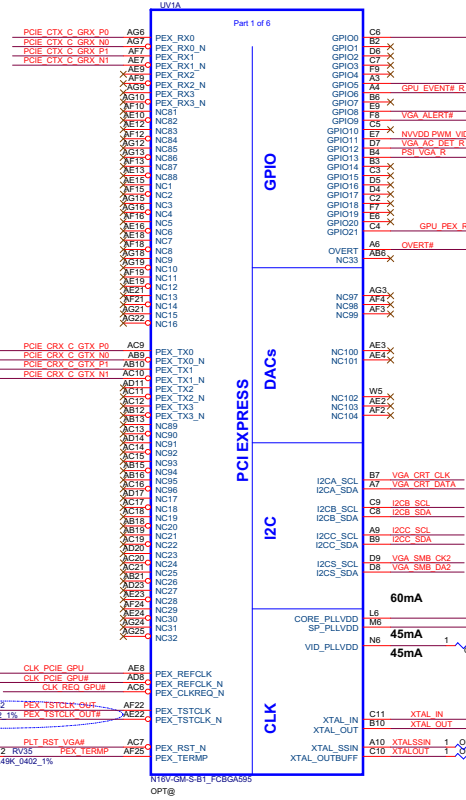
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

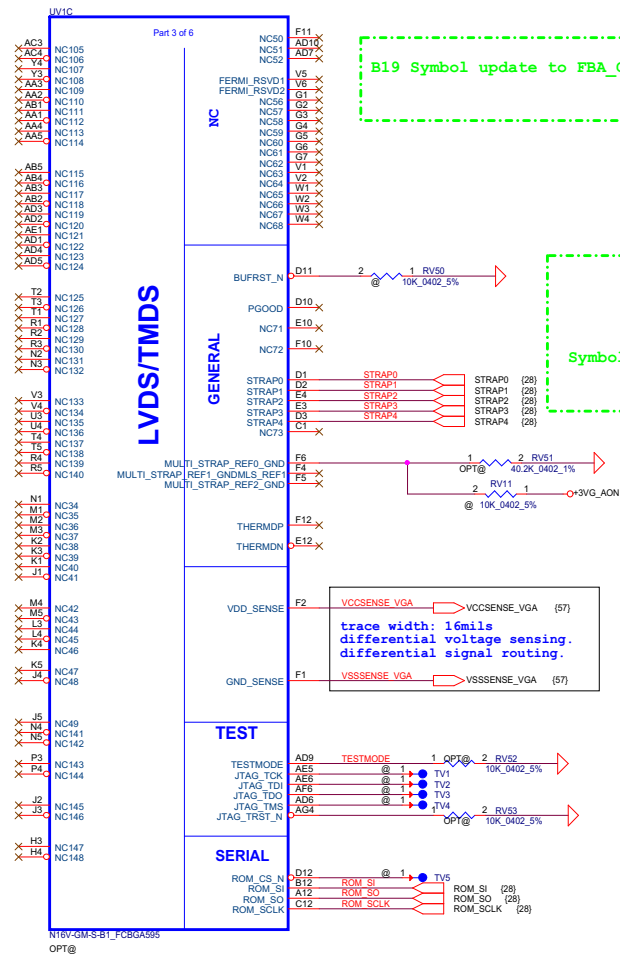
RV1 2 0.0402 5% FB_G08_EN_R
RV2 2 0.0402 5% GPU_EVENT#

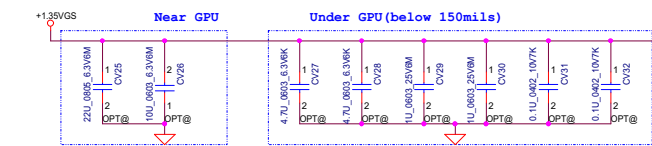
(6) PCIE_CRX_GTX_N0.1
(6) PCIE_CRX_GTX_P0.1
(6) PCIE_CTX_C_GRX_N0.1
(6) PCIE_CTX_C_GRX_P0.1



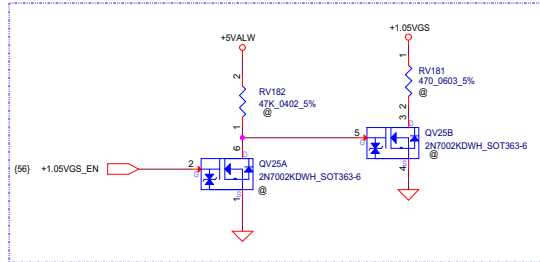
Connect to CPU GPIO



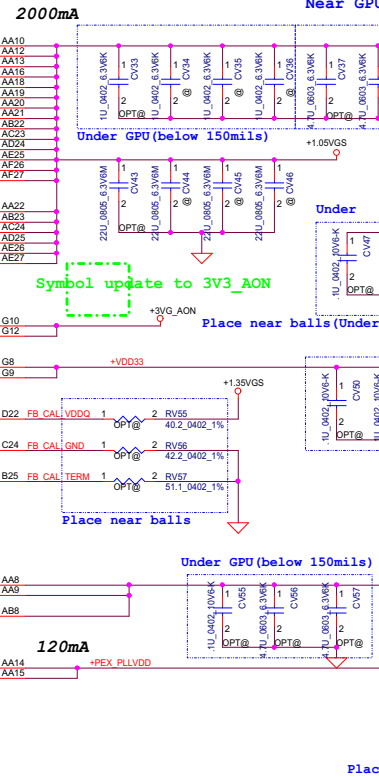
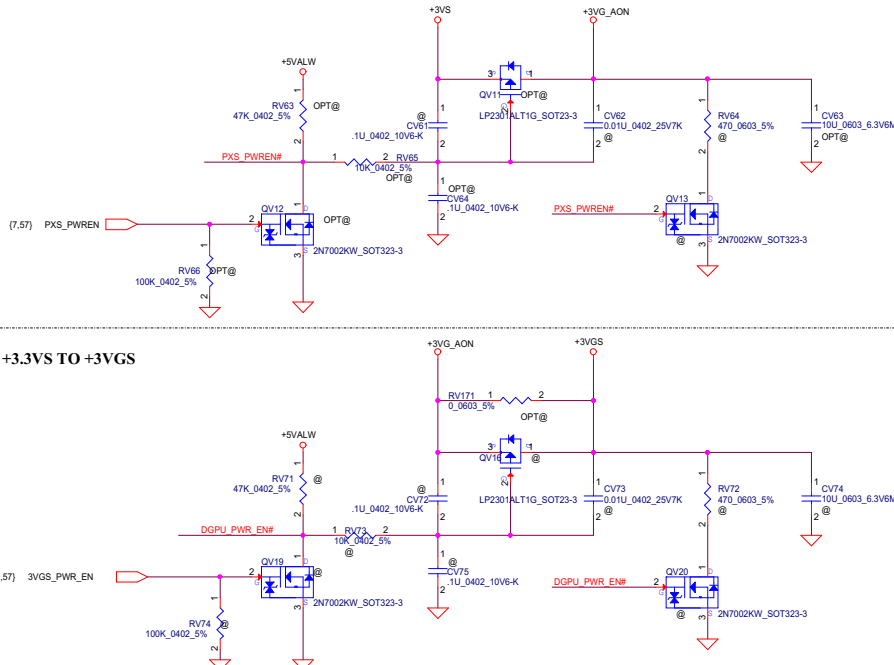




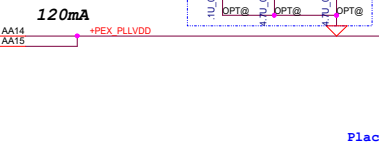
Symbol update to FBVDDQ_AON
H24/H26/J21/K21



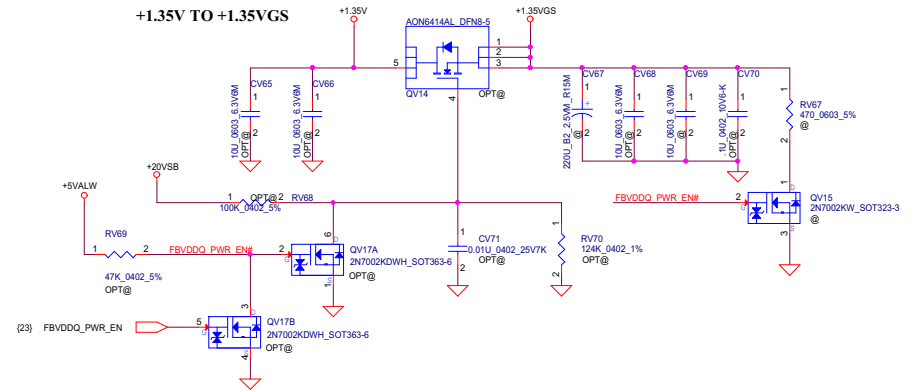
+3.3VS TO +3VG_AON



Symbol update to 3V3_AON



+1.35V TO +1.35VGS

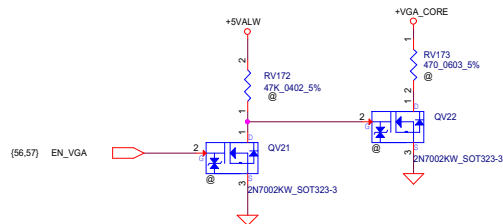
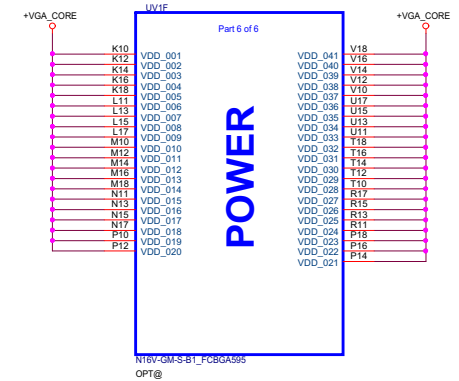
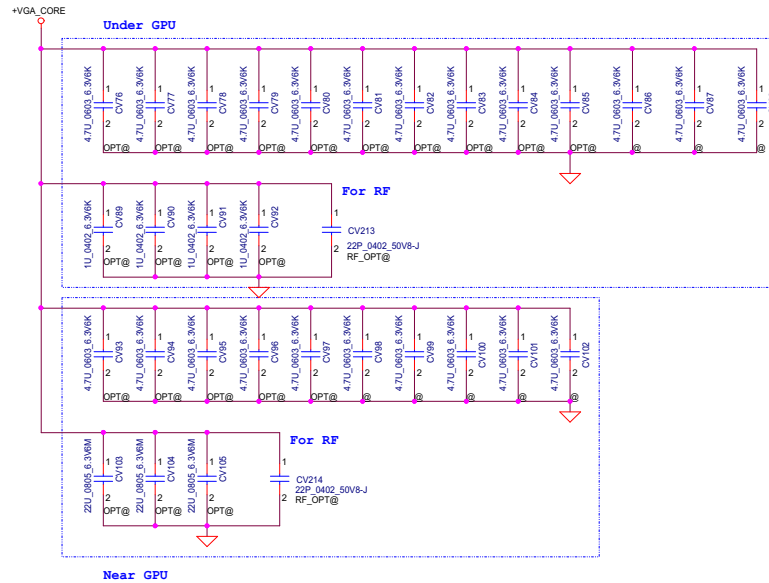
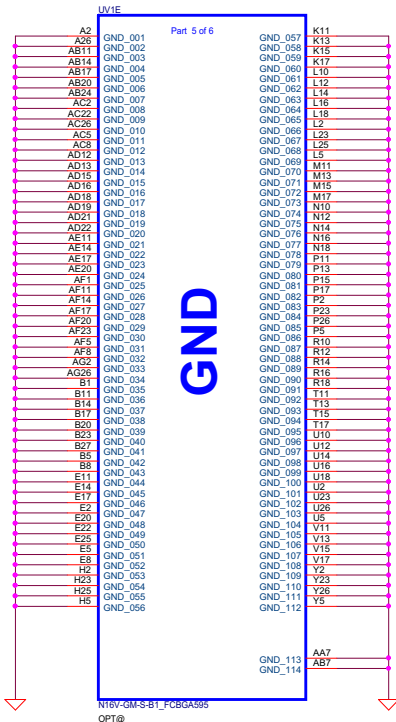


POWER

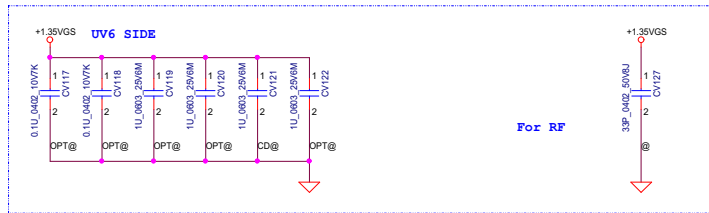
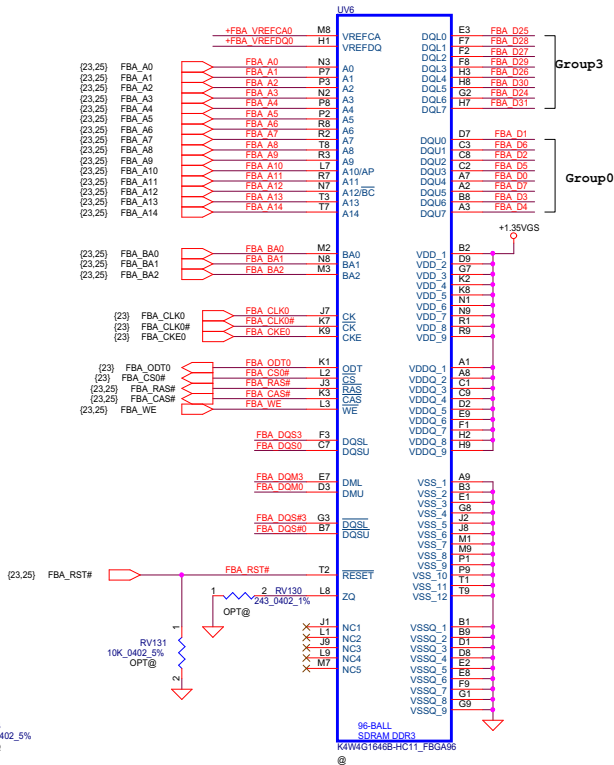
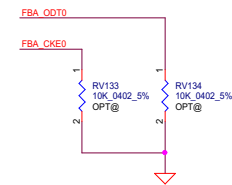
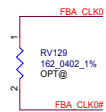
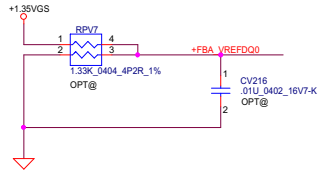
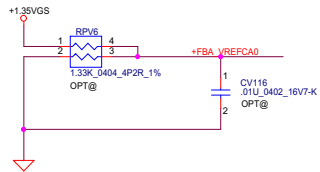
PEX_IOVDD/Q Decoupling

MLCC	N15V-GM	N15S-GT
1.0uF	4	1
4.7uF	2	1
10uF	4	1
22uF	4	1

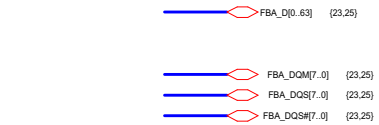
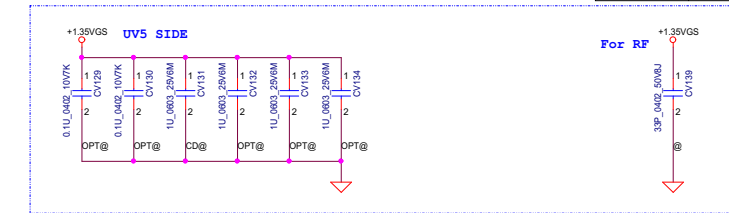
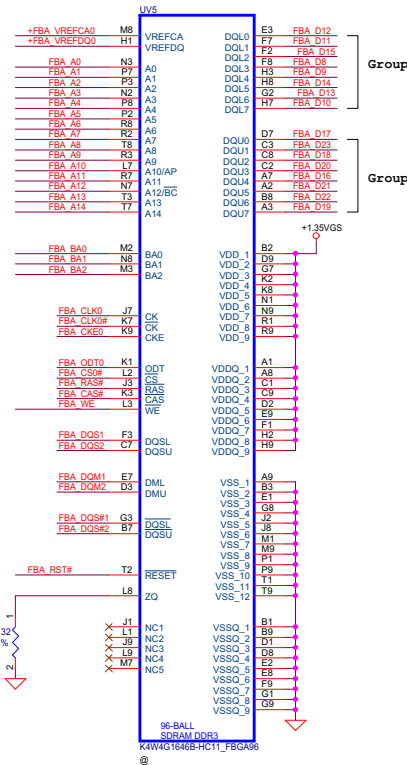
CALIBRATION PIN	DDR3
FB_CAL x PD_VDDQ	40.2Ohm
FB_CAL x PU_GND	42.2Ohm
FB_CAL x TERM_GND	51.1Ohm



at least 16 mils width/optimal)
20 mils spacing to other signals /planes



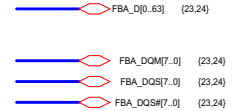
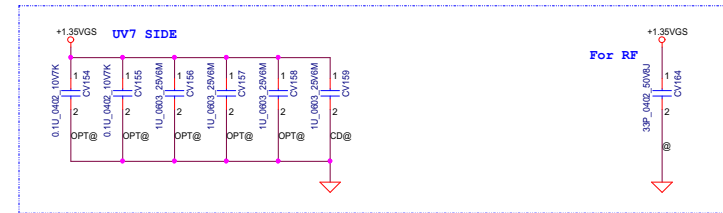
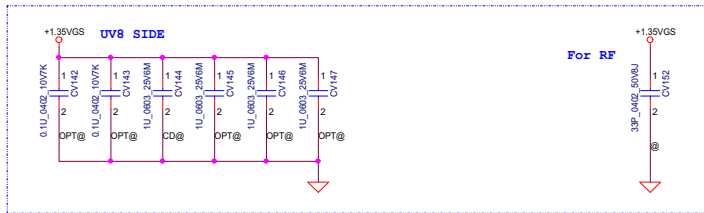
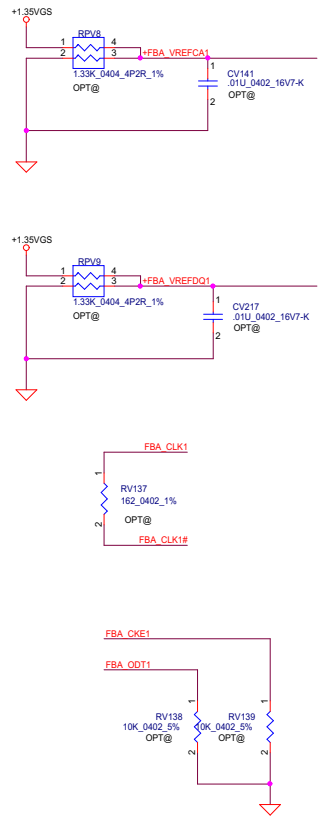
For RF



CMD mapping mod Mode D

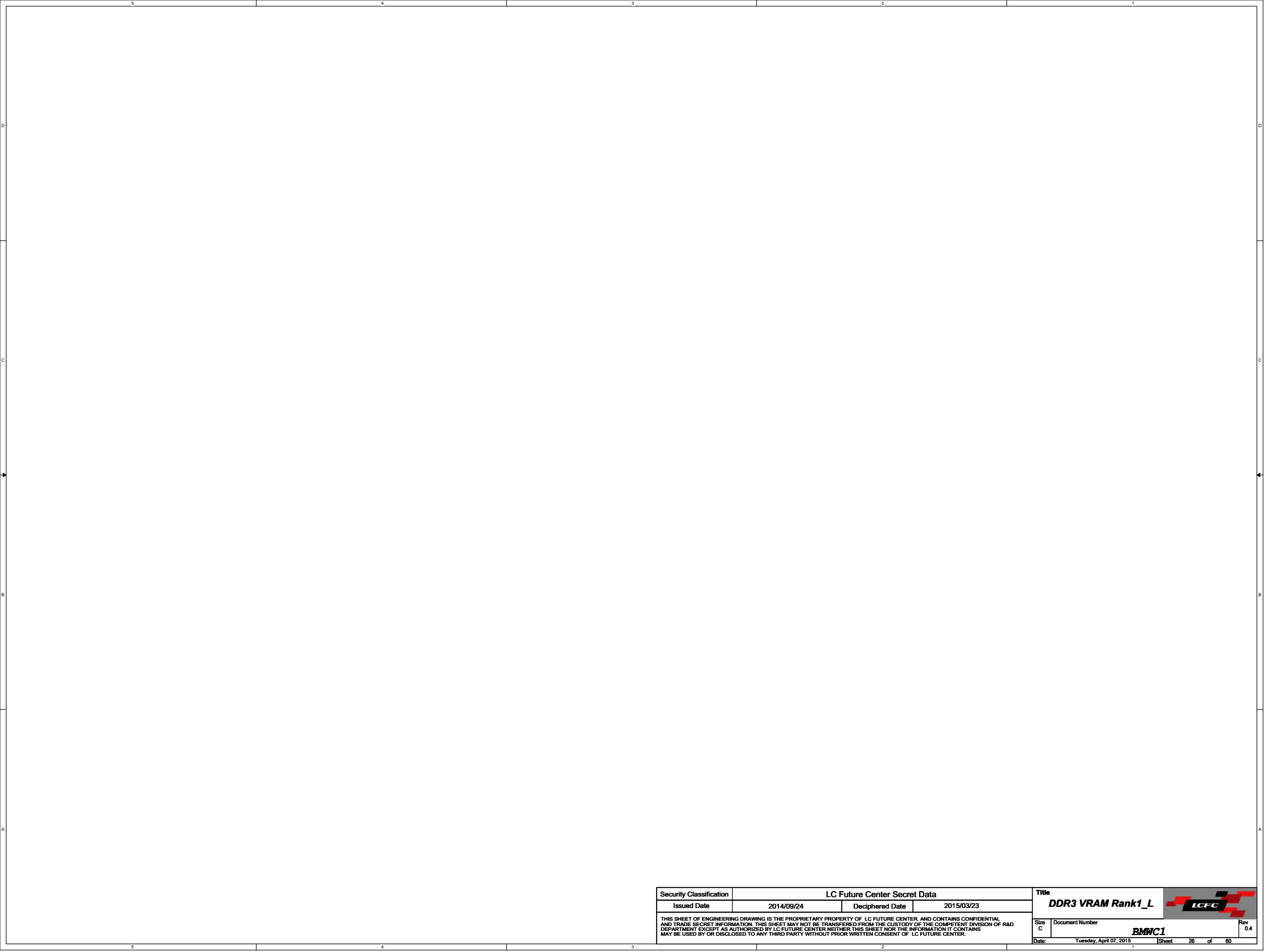
Address	Rank0	Rank1
FbX_CMD0	CS0#	32..63
FbX_CMD1		
FbX_CMD2	ODT0	
FbX_CMD3	CKE0	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE	WE
FbX_CMD14	A15	A15
FbX_CMD15	CAS#	CAS#
FbX_CMD16	CS1#	
FbX_CMD17		
FbX_CMD18		ODT1
FbX_CMD19		CKE1
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5
FbX_CMD25	A3	A3
FbX_CMD26	BA2	BA2
FbX_CMD27	BA1	BA1
FbX_CMD28	A12	A12
FbX_CMD29	A10	A10
FbX_CMD30	RAS#	RAS#
FbX_CMD31		
FbX_CMD32		
FbX_CMD33		
FbX_CMD34	DBG0	
FbX_CMD35	DBG1	

at least 16 mils width(optimal)
20 mils spacing to other signals /planes



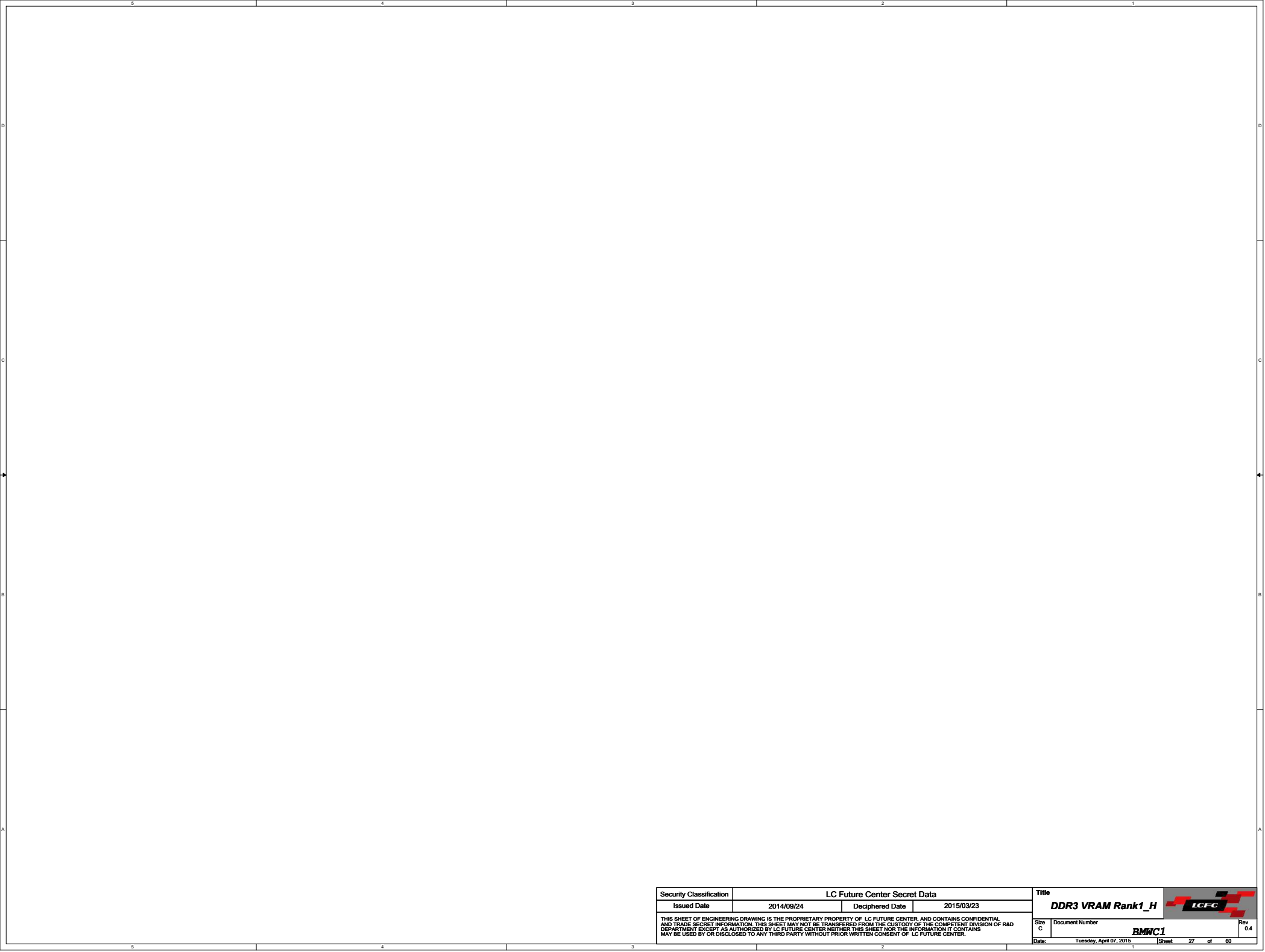
CMD mapping mod Mode D

Rank0		Rank1	
Address	0..31	32..63	
FBx_CMD0	CS0#		
FBx_CMD1			
FBx_CMD2	ODT0		
FBx_CMD3	CKE0		
FBx_CMD4	A14	A14	
FBx_CMD5	RST	RST	
FBx_CMD6	A9	A9	
FBx_CMD7	A7	A7	
FBx_CMD8	A2	A2	
FBx_CMD9	A0	A0	
FBx_CMD10	A4	A4	
FBx_CMD11	A1	A1	
FBx_CMD12	BA0	BA0	
FBx_CMD13	WE	WE	
FBx_CMD14	A15	A15	
FBx_CMD15	CAS#	CAS#	
FBx_CMD16		CS1#	
FBx_CMD17			
FBx_CMD18		ODT1	
FBx_CMD19		CKE1	
FBx_CMD20	A13	A13	
FBx_CMD21	A8	A8	
FBx_CMD22	A6	A6	
FBx_CMD23	A11	A11	
FBx_CMD24	A5	A5	
FBx_CMD25	A3	A3	
FBx_CMD26	BA2	BA2	
FBx_CMD27	BA1	BA1	
FBx_CMD28	A12	A12	
FBx_CMD29	A10	A10	
FBx_CMD30	RAS#	RAS#	
FBx_CMD31			
FBx_CMD32			
FBx_CMD33			
FBx_CMD34	DBG0		
FBx_CMD35	DBG1		



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	DDR3 VRAM Rank1_L	
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D

D

C

C

B

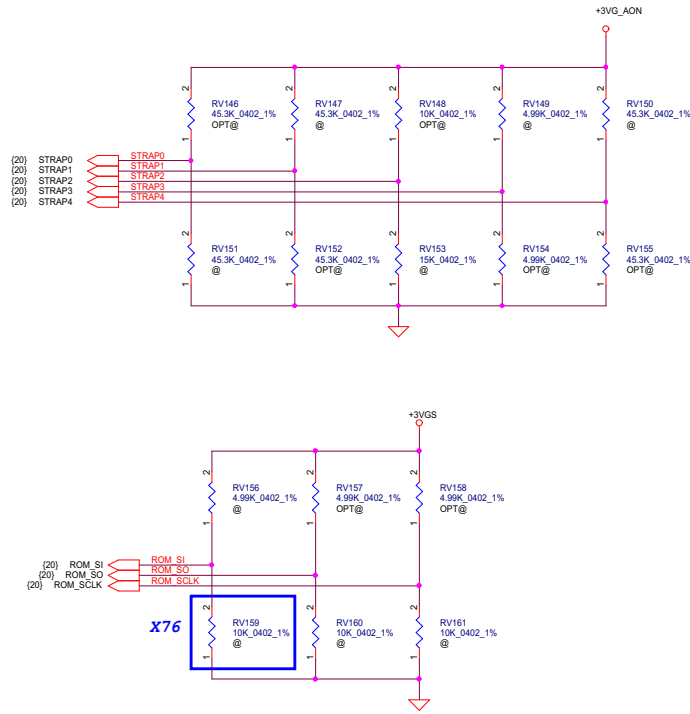
B

A

A

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2014/09/24	Deciphered Date	2015/03/23	DDR3 VRAM Rank1_H	
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				Date: Tuesday, April 07, 2015	Rev 0.4
				Sheet 27	of 60





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD03449918J		
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
SD03424928J		
30.1K	1101	0101
SD03430128J		
34.8K	1110	0110
SD03434828J		
45.3K	1111	0111
SD03445328J		

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

GPU		FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16V-GM	Hynix 900MHz	H5TC4G63AFR-11C	0xE	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K
		256M x 16 0xE	PU 34.8K							
	Micron 900MHz	MT41J256M16HA-093G:E	0xD							
		256M x 16 0xD	PU 30.1K							
	Hynix 900MHz	H5TC2G63FFR-11C	0xB							
		128M x 16 0xB	PU 20K							
	Micron 900MHz	MT41J128M16JT-093G	0x8							
		128M x 16 0x8	PU 4.99K							
	Samsung 900MHz	K4W2G1646Q-BC1A	0x7							
		128M x 16 0x7	PD 45.3K							

VRAM	X76	VRAM P/N
Samsung	X7606012101	SA00005SH40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00

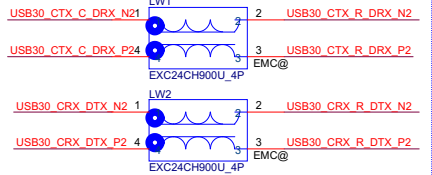


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Issued Date		2014/09/24		Deciphered Date					
		2015/03/23							
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				Custom		BMWC1		0.4	
Date:				Tuesday, April 07, 2015		Sheet		29 of 59	



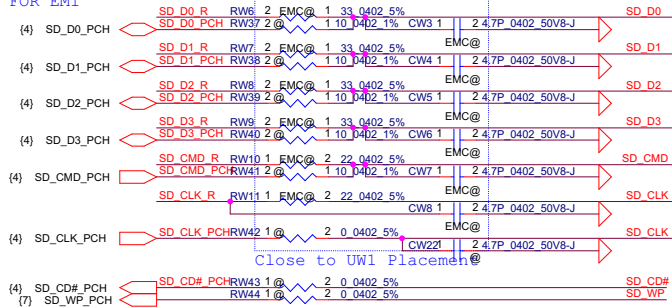
(8) USB30_CTX_DRX_N2 1U_0402_10V6-K CW25 1 2USB30_CTX_C_DRX_N2 1 RW1 @ 2 0.0402_5% USB30_CTX_R_DRX_N2
(8) USB30_CTX_DRX_P2 1U_0402_10V6-K CW26 1 2USB30_CTX_C_DRX_P2 1 RW2 @ 2 0.0402_5% USB30_CTX_R_DRX_P2

(8) USB30_CRX_DTX_N2 1U_0402_10V6-K RW3 1 @ 2 0.0402_5% USB30_CRX_R_DTX_N2
(8) USB30_CRX_DTX_P2 1U_0402_10V6-K RW4 1 @ 2 0.0402_5% USB30_CRX_R_DTX_P2

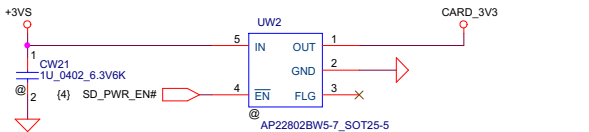


FOR EMI

FOR EMI

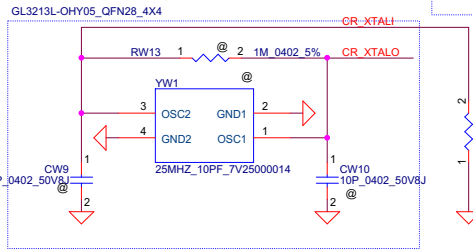
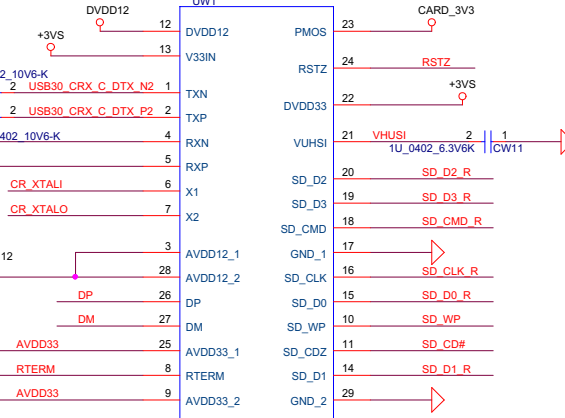


Close to UW1 Placement

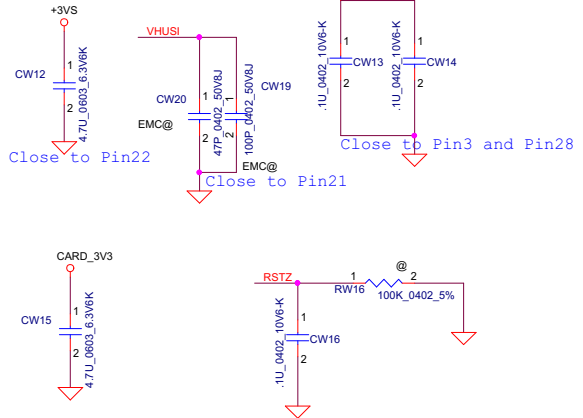


Low Active 2A

USB30_CRX_R_DTX_N2 1U_0402_10V6-K CW1 1 2 USB30_CRX_C_DTX_N2 1
USB30_CRX_R_DTX_P2 CW2 1 2 USB30_CRX_C_DTX_P2 2
USB30_CTX_R_DRX_N2 1U_0402_10V6-K
USB30_CTX_R_DRX_P2



FOR ESD Close to Connector



Close to Pin22

Close to Pin21

CARD_3V3

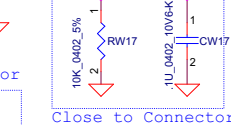
CW15

Close to Pin3 and Pin28

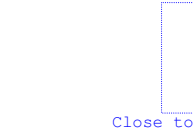
Close to Pin21

CARD_3V3

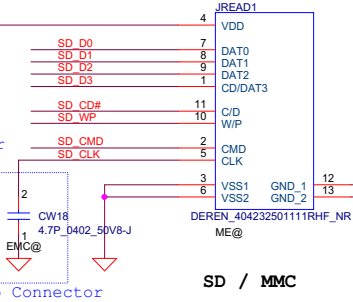
CW16



Close to Connector

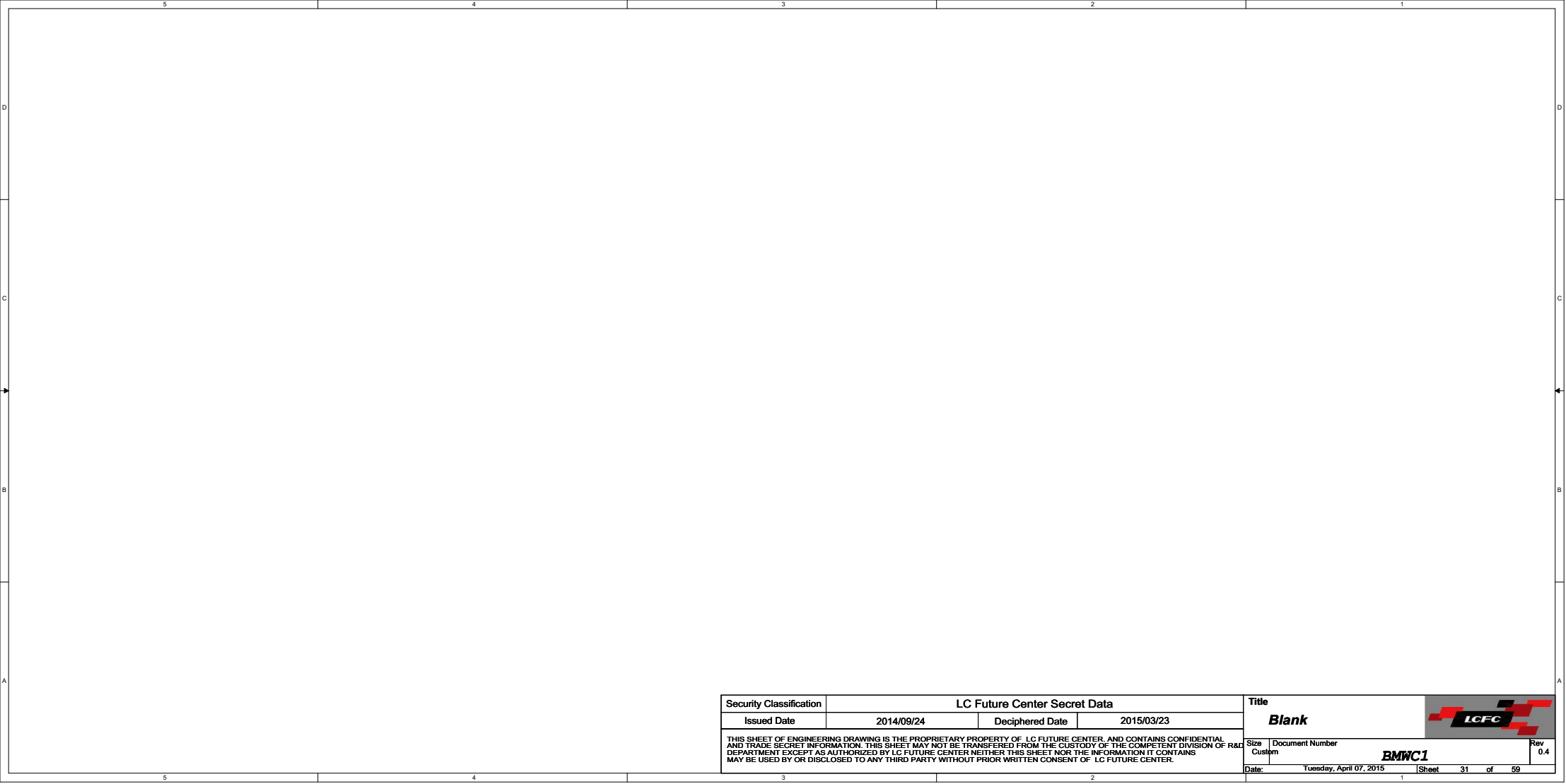


Close to Connector

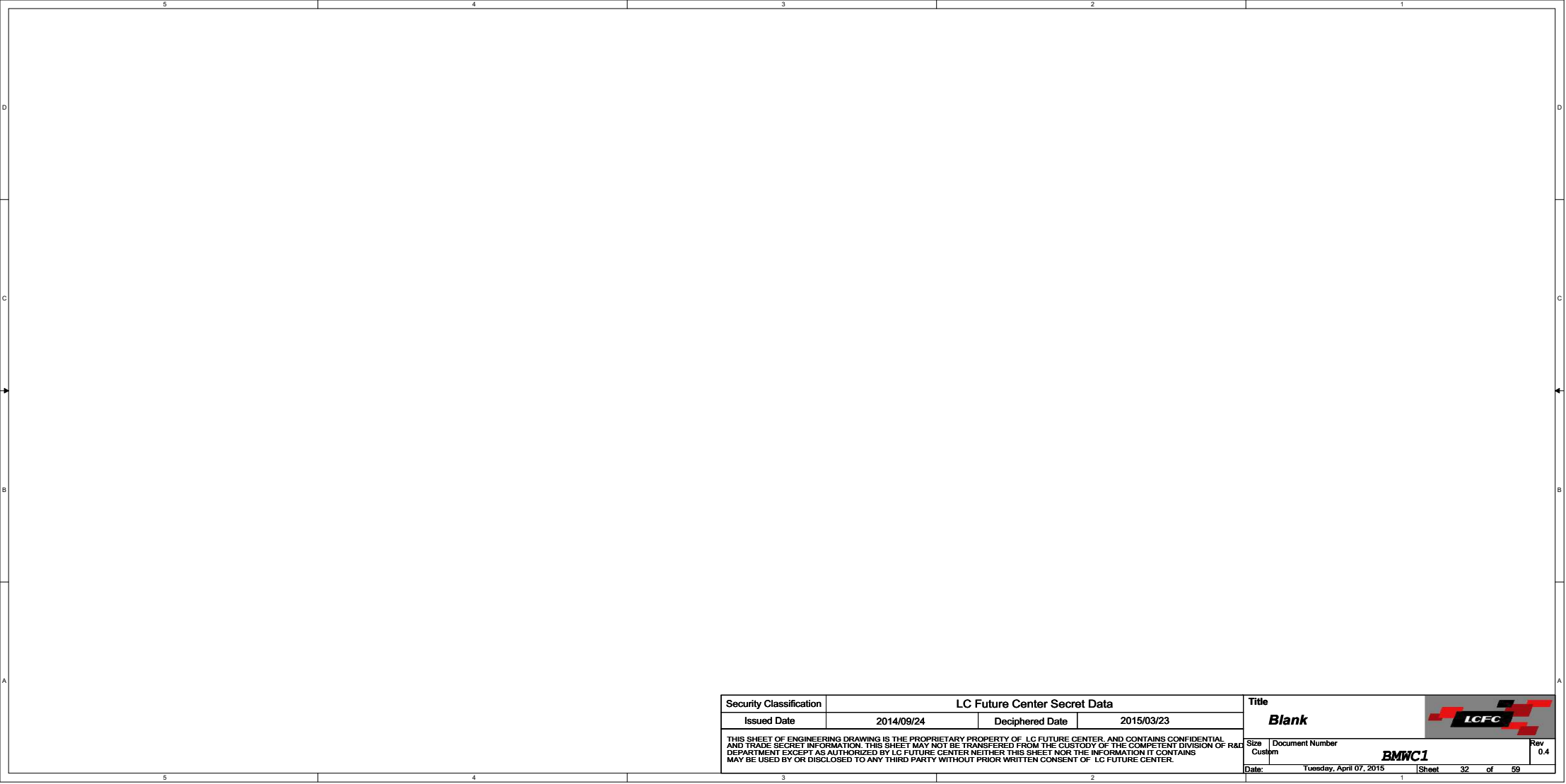


SD / MMC

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		Custom		0.4	
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		59			



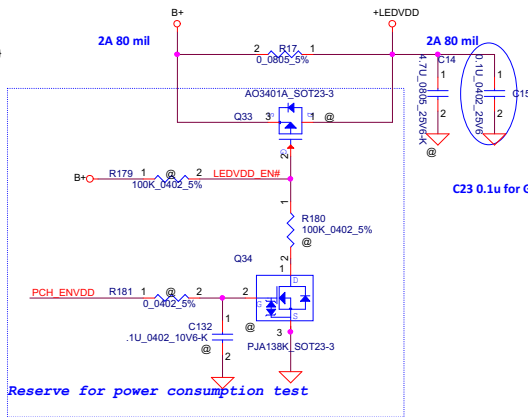
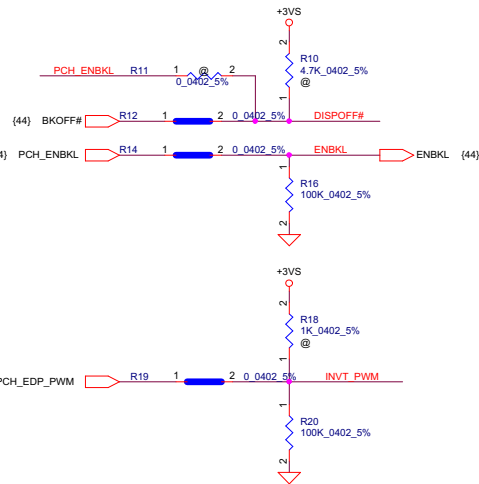
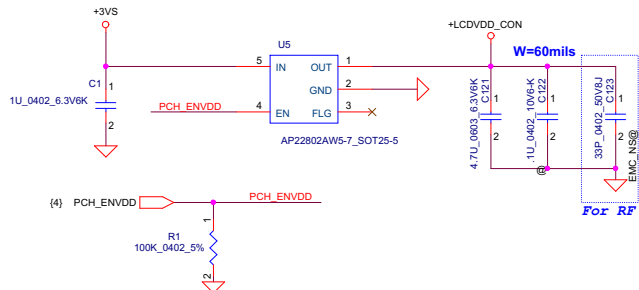
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Date:		Tuesday, April 07, 2015		Sheet		32 of 59		

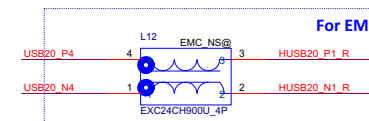
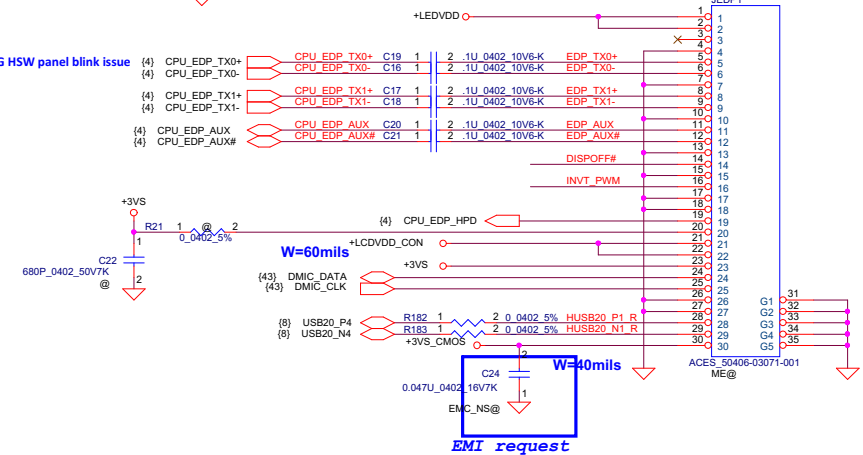
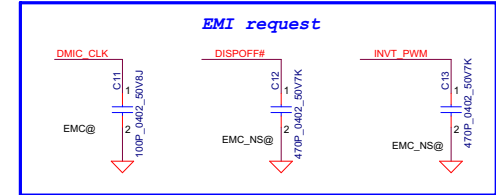
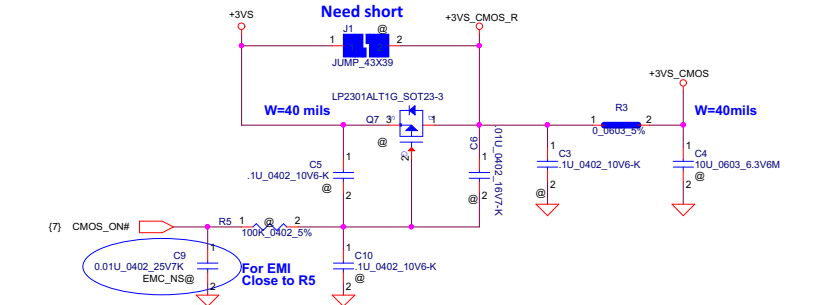
LCD POWER CIRCUIT

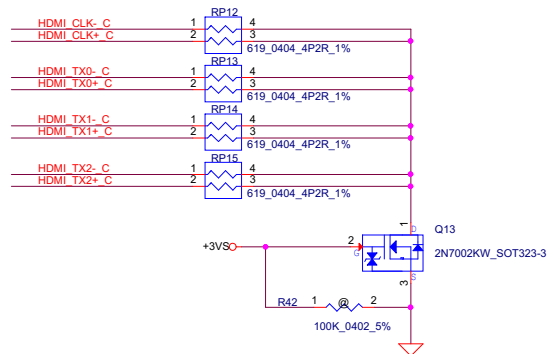
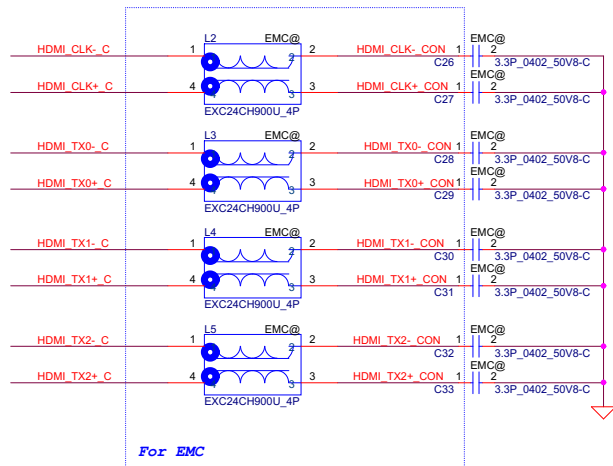
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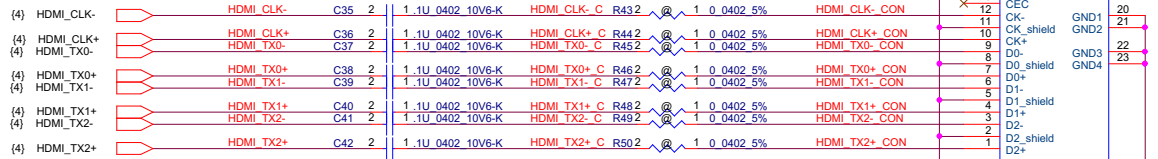
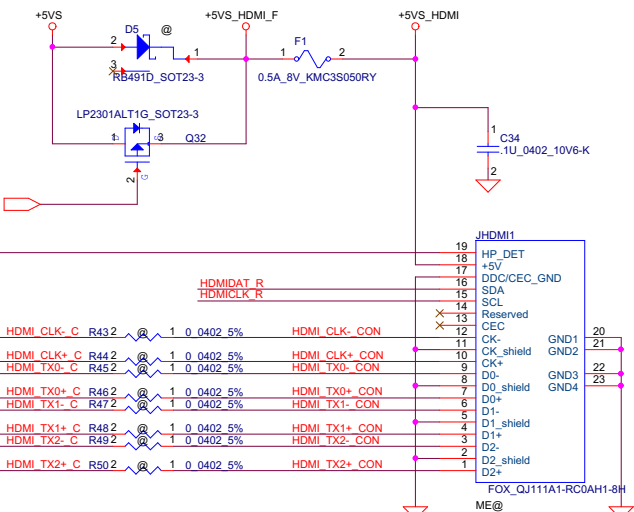
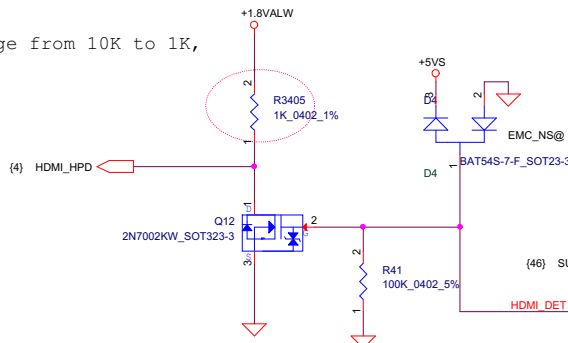
CMOS Camera

Need short

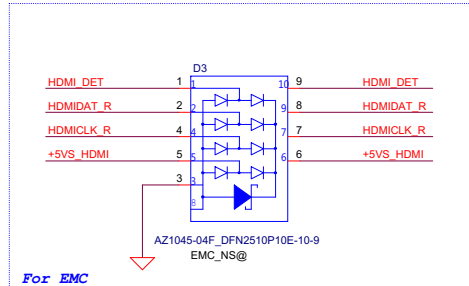
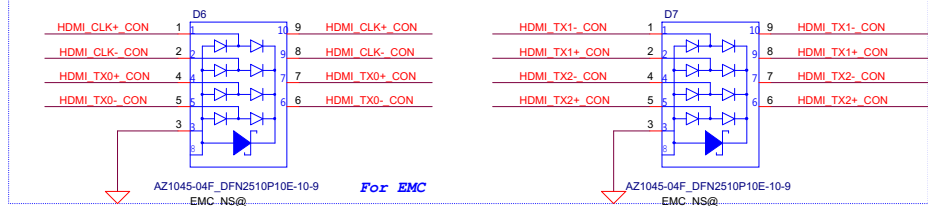


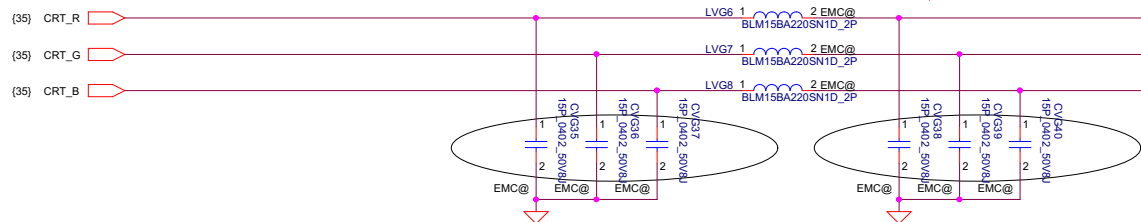
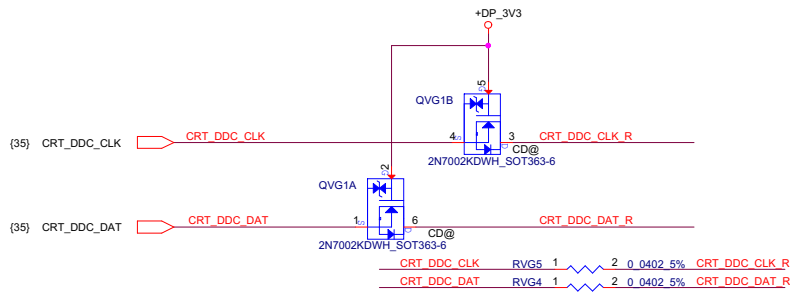


R4602 change from 10K to 1K,
as Vienna

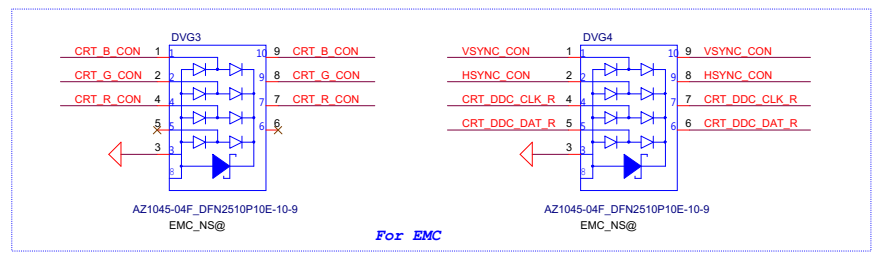
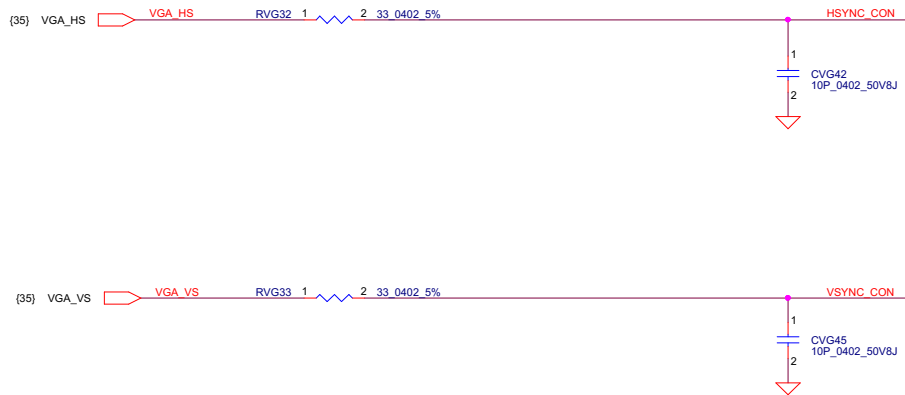
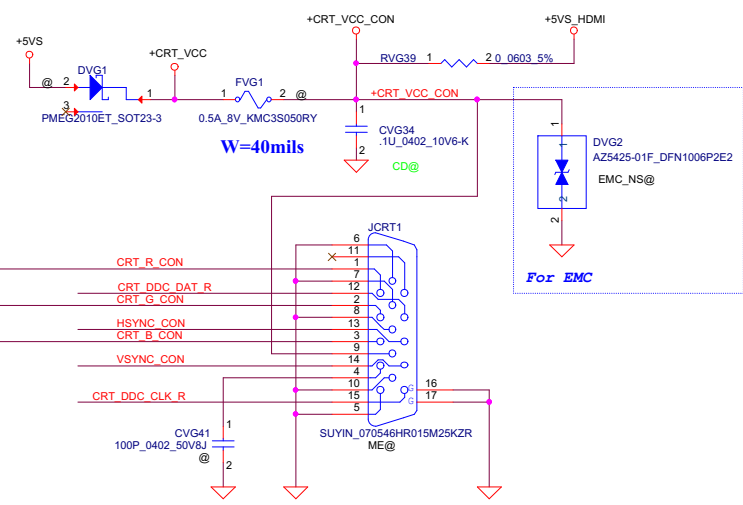


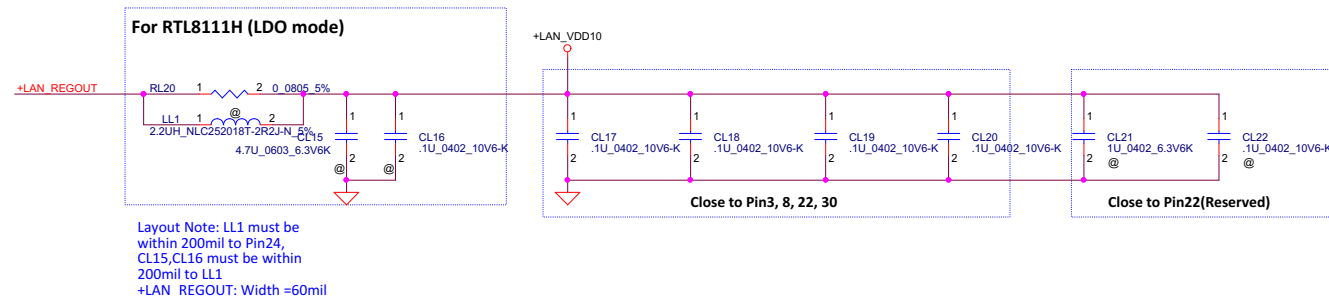
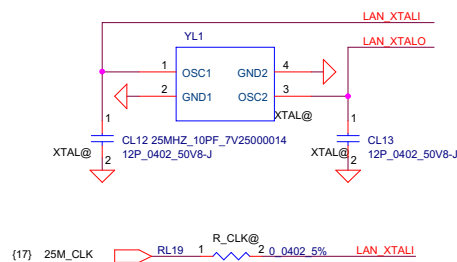
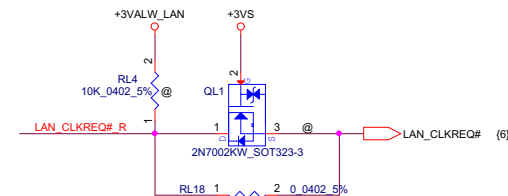
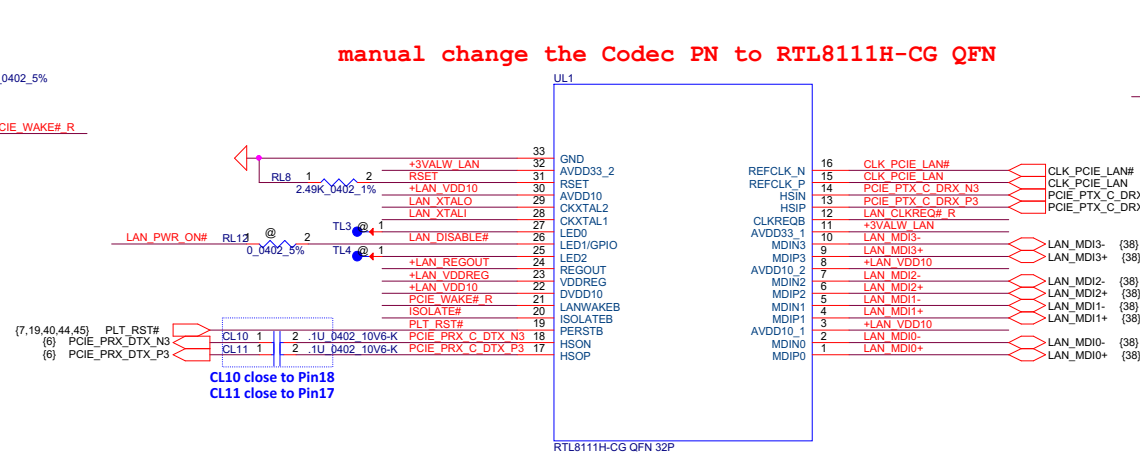
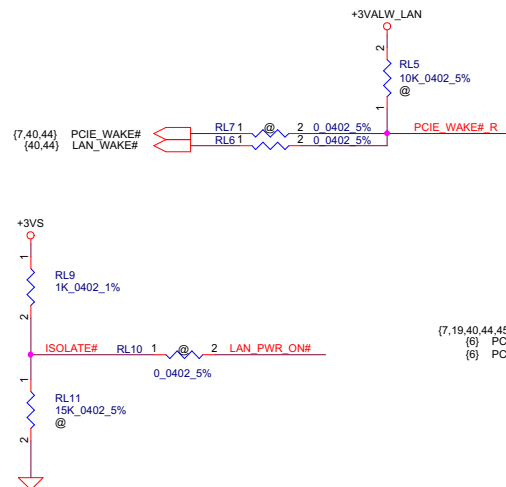
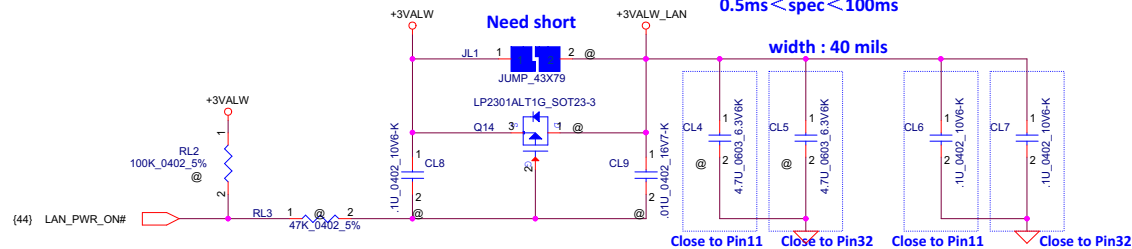
Close to JHDMI1





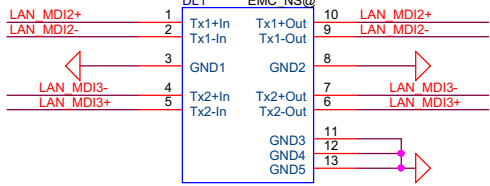
CRT Connector



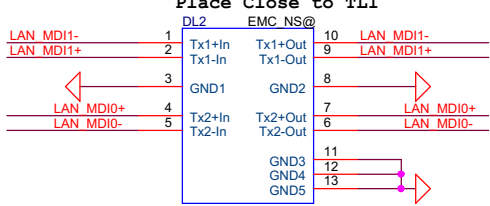


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DL1/DL2
1'S PN:SC400007R00

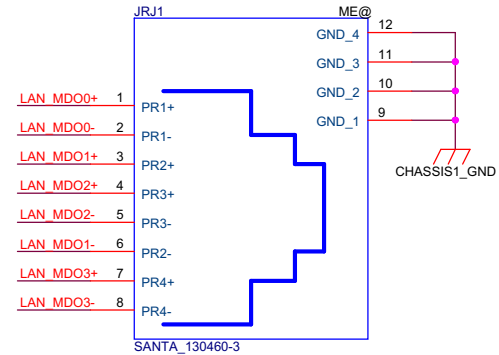
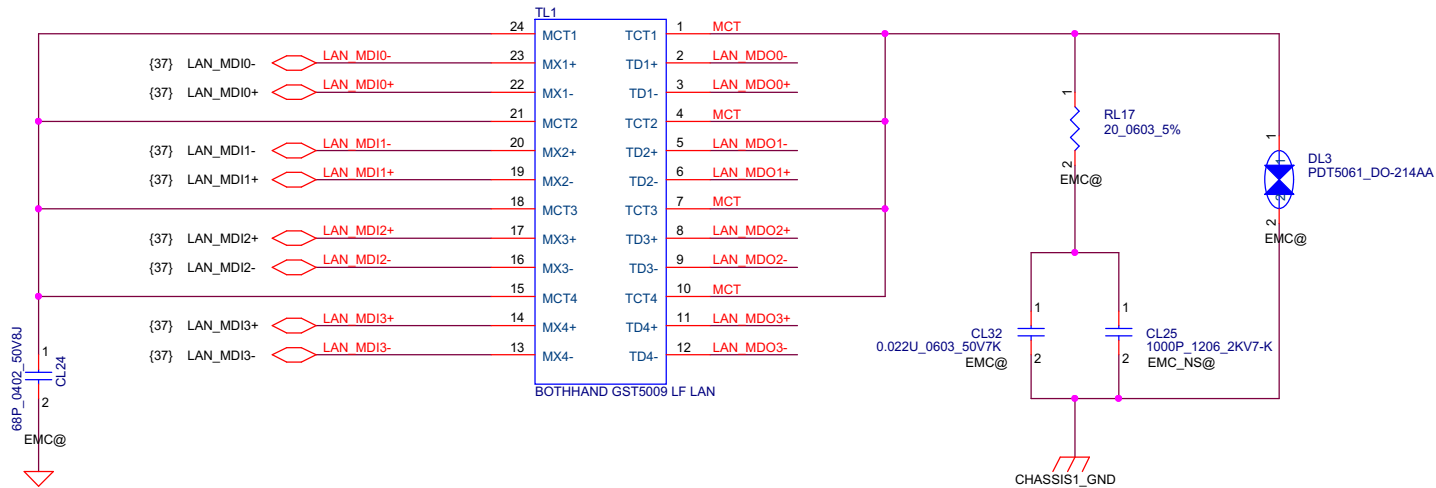
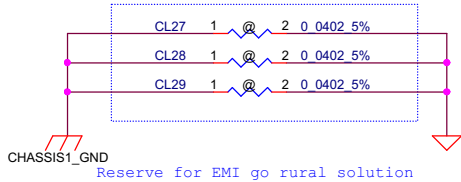


RCLAMP3374N.TCT_SLP3020N10-10

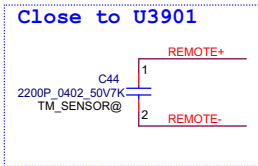


RCLAMP3374N.TCT_SLP3020N10-10

Place Close to TL2

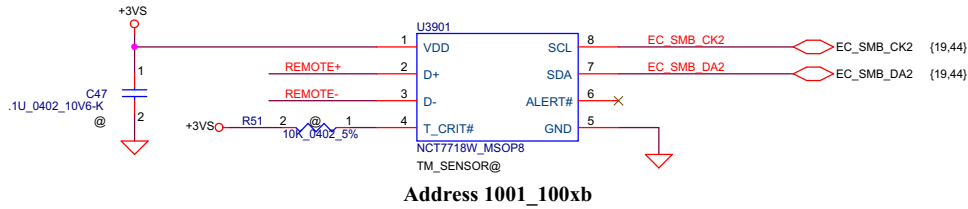


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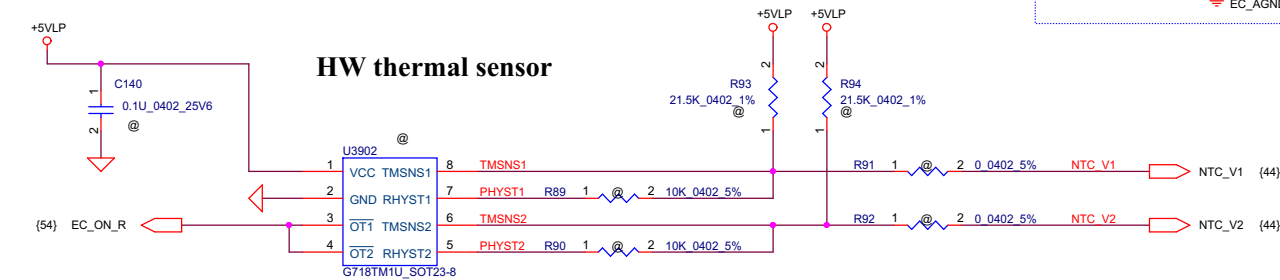


REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

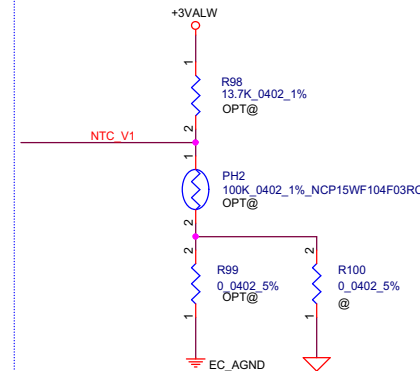


HW thermal sensor

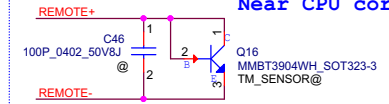


over temperature threshold:
 $RSET=3 \times RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST=(RSET \times RTML) / (3 \times RTML - RSET)$
56+/-30C

Near GPU&VRAM

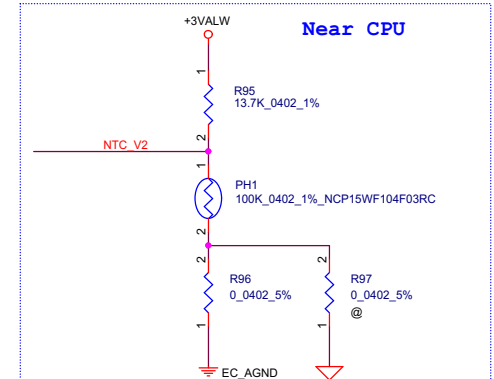


Near CPU core

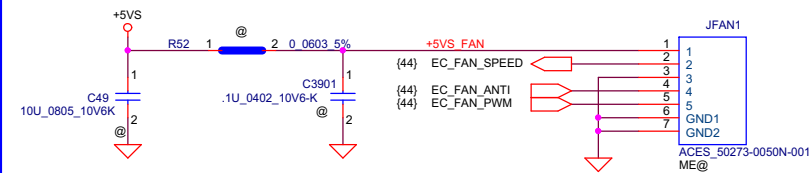


Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

Near CPU



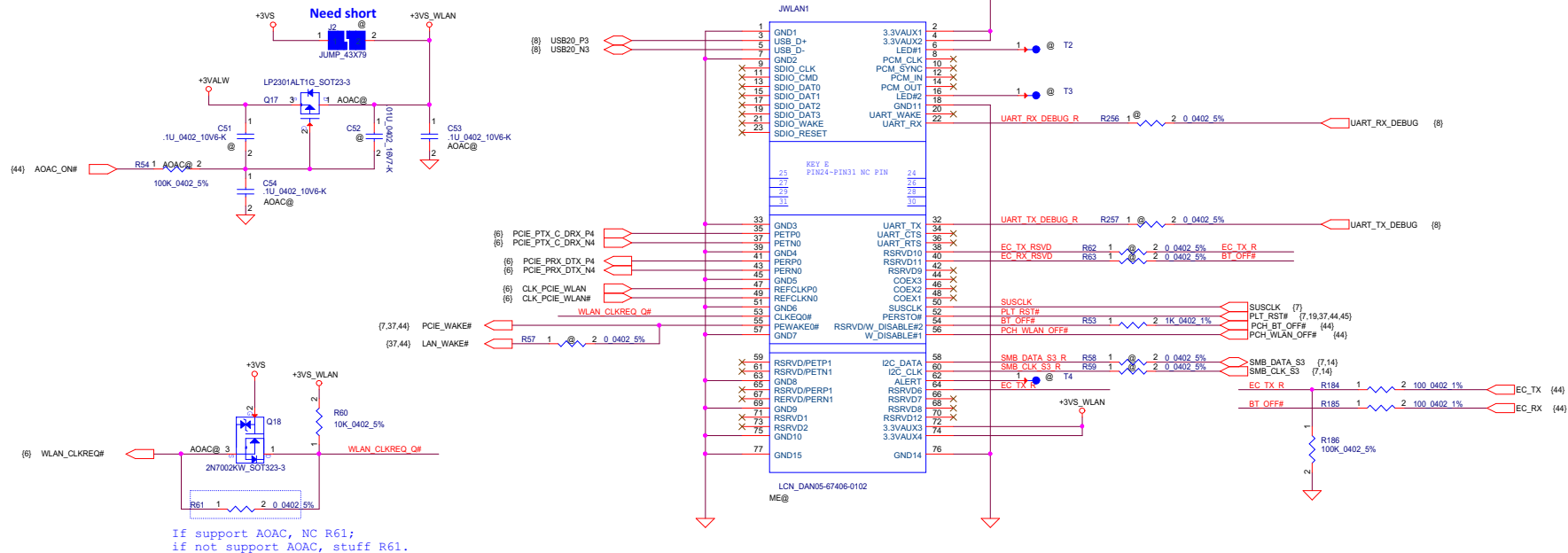
FAN Conn



JFAN1 Pin defin need check other G

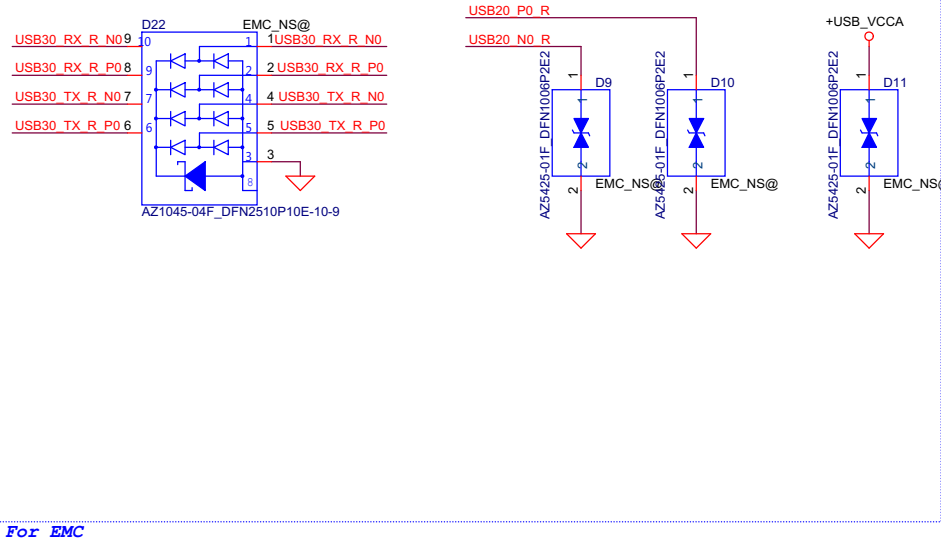
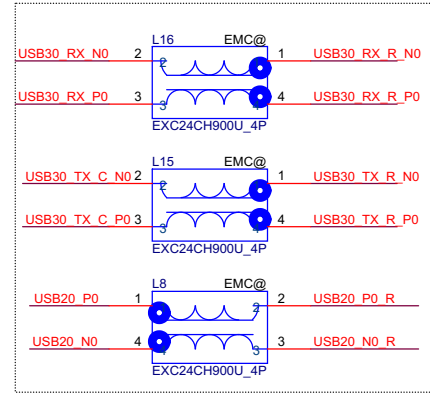
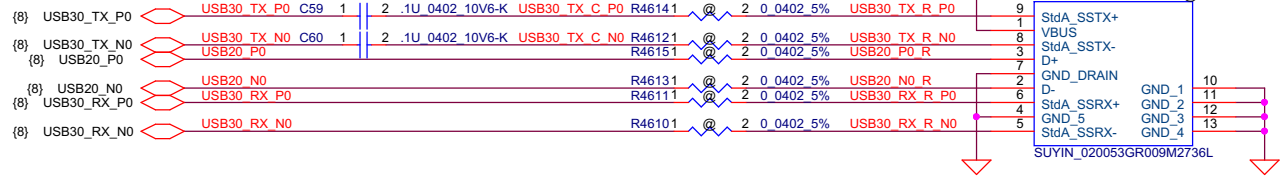
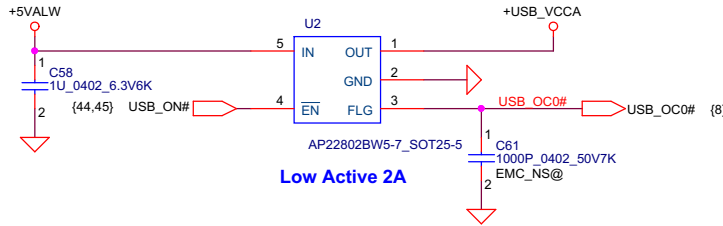
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Mini-Express Card(WLAN/WiMAX)



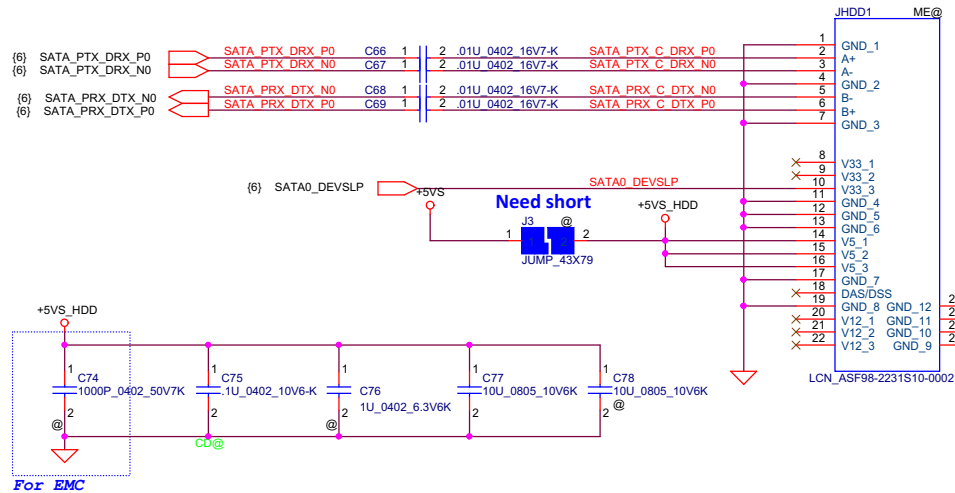
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LEFT SIDE USB3.0 PORT X1

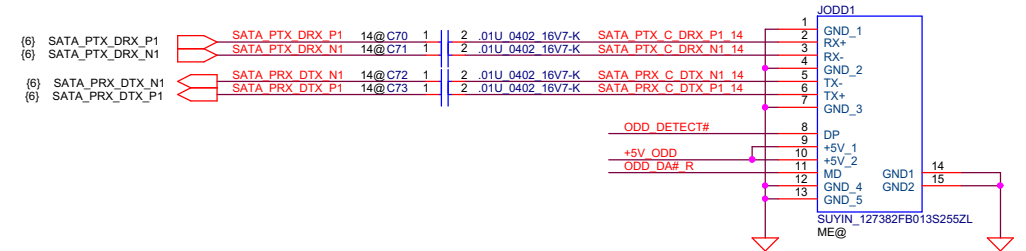


For EMC

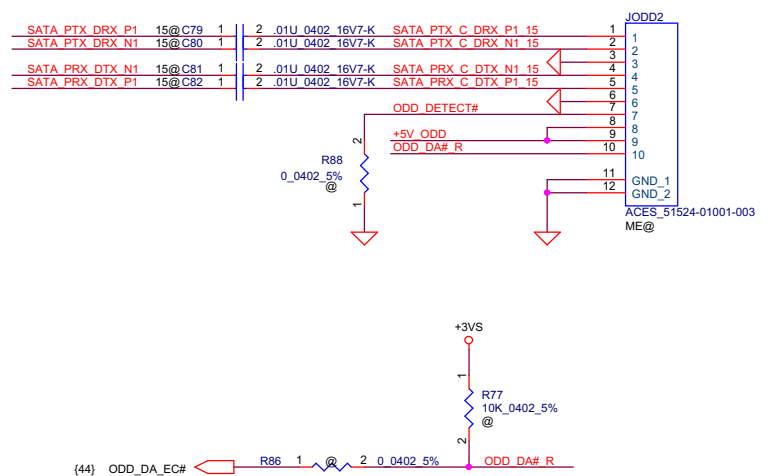
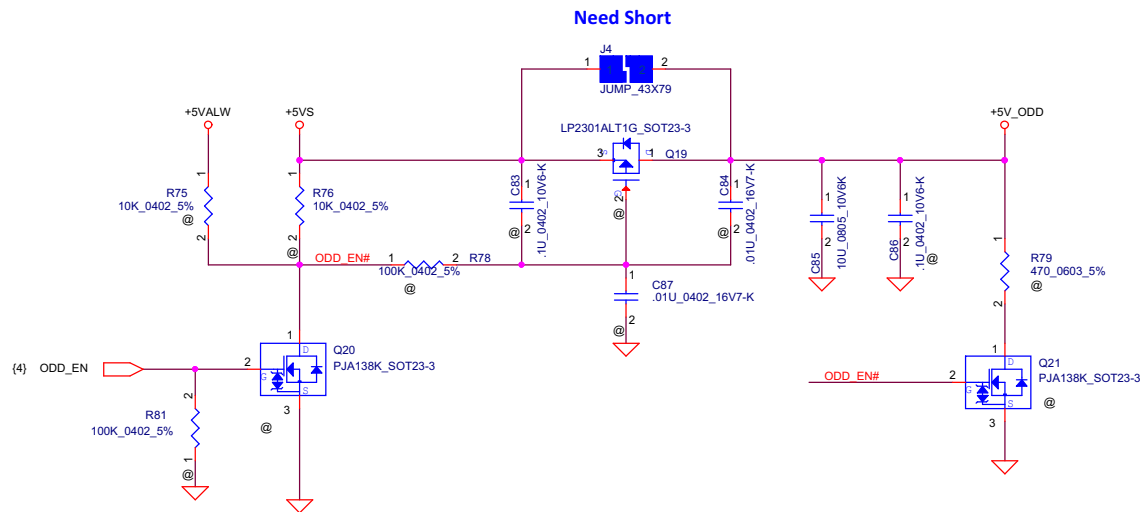
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Issued Date	2014/09/24	Deciphered Date	2015/03/23	USB2.0/USB3.0 PORT (LEFT)		
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SATA HDD Conn.

FOR 14"
SATA ODD Conn.

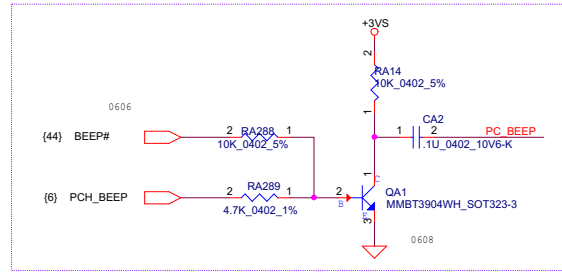


FOR 15"
SATA ODD FFC Conn

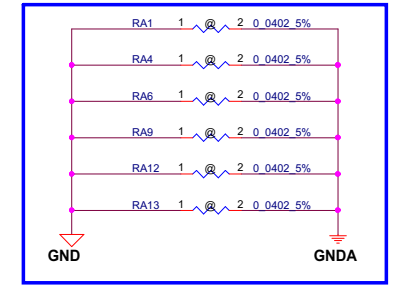
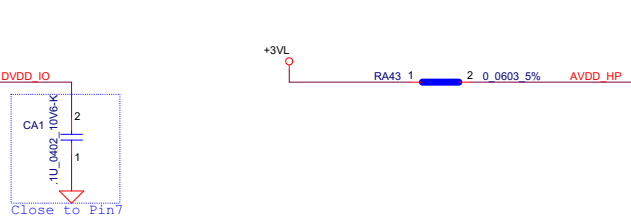
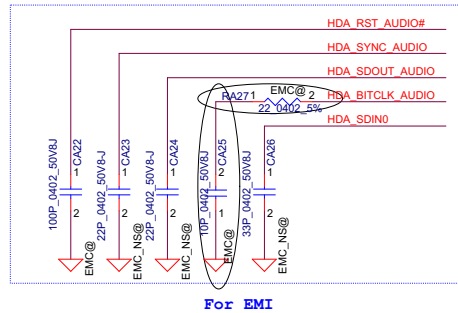
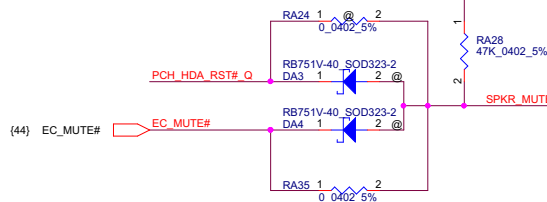
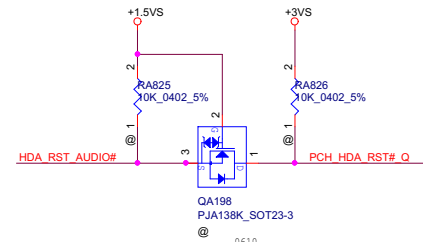
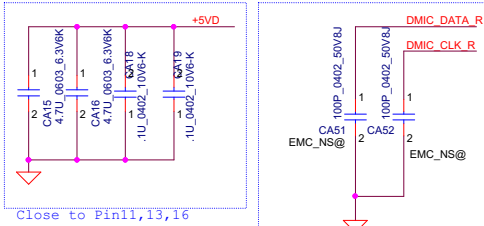
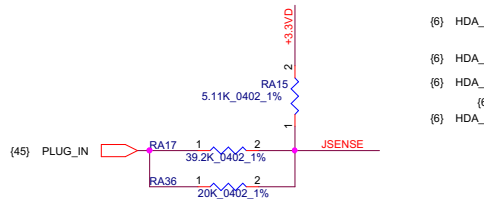


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Same as Vienna



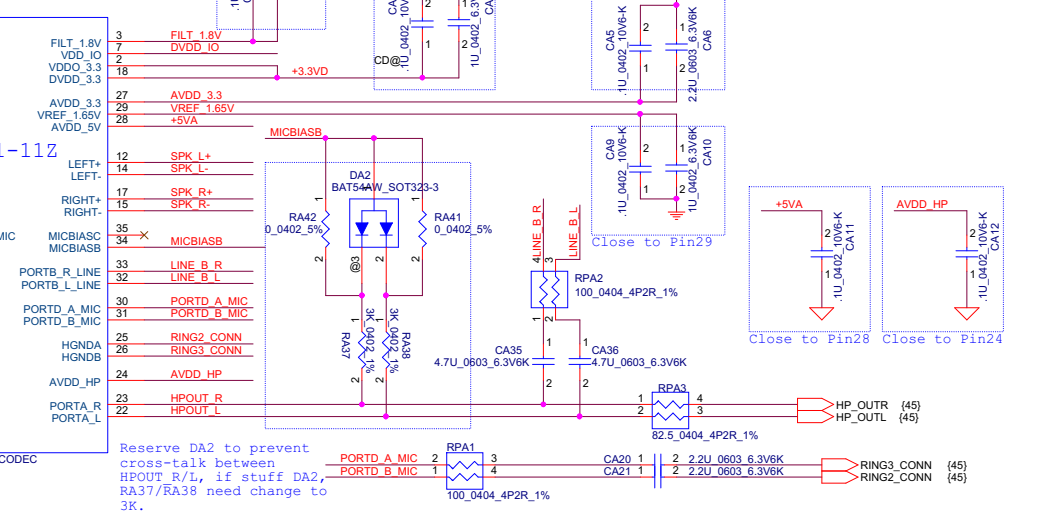
manual change the Codec PN to CX11802-33Z



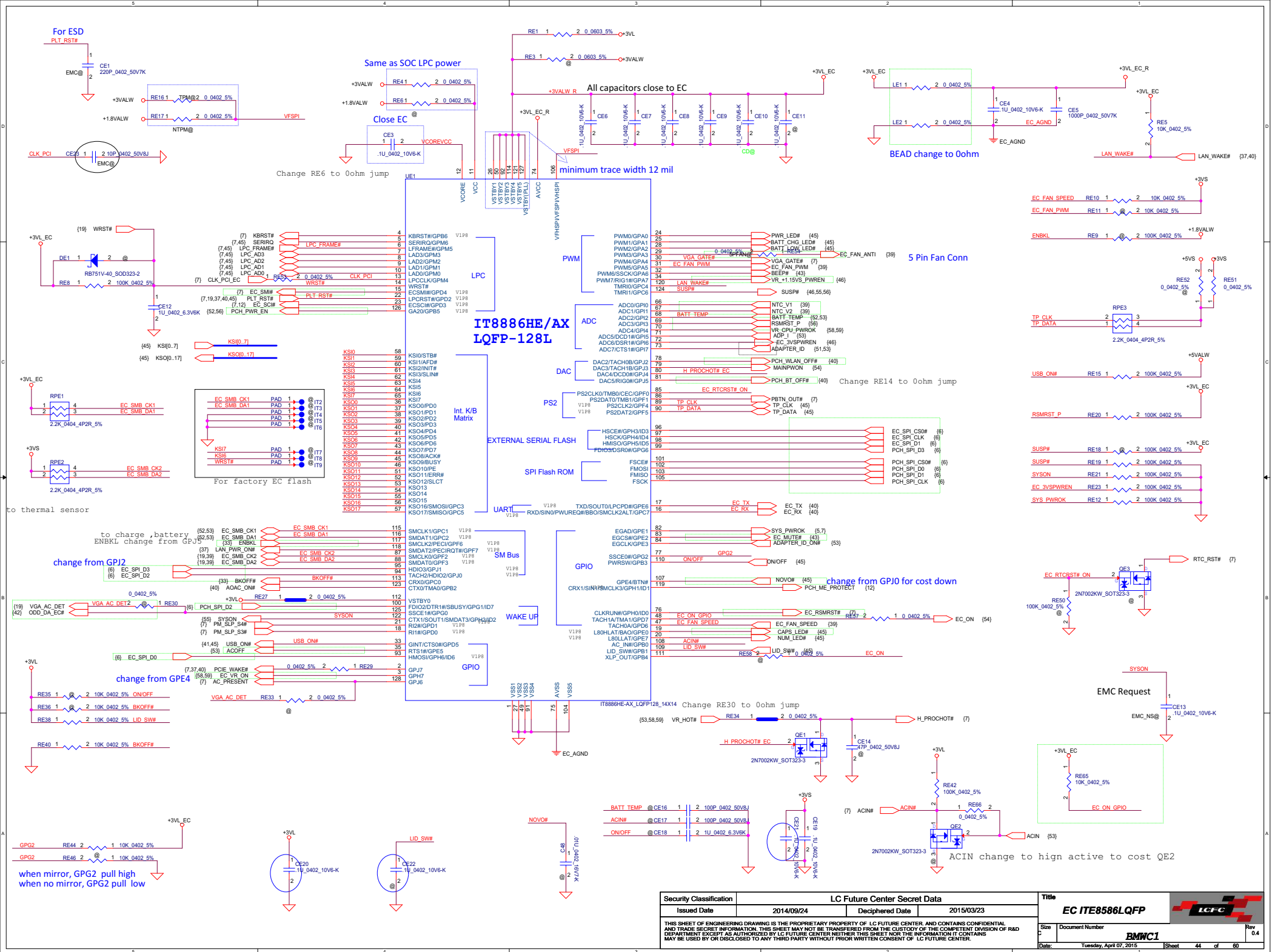
Close to Pin3

CA16 close to Pin18
CA17 close to Pin2

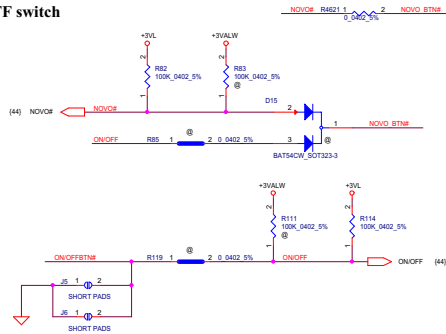
Close to Pin27



Reserve DA2 to prevent cross-talk between HPOUT R/L, if stuff DA2, RA37/RA38 need change to 3K.



ON/OFF switch

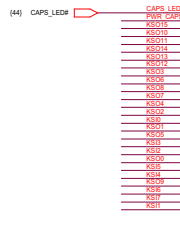


TP/B Connector

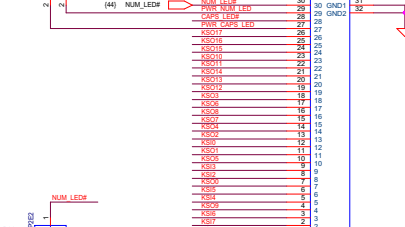
K/B Connector



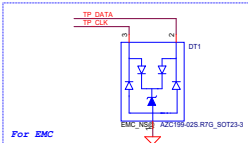
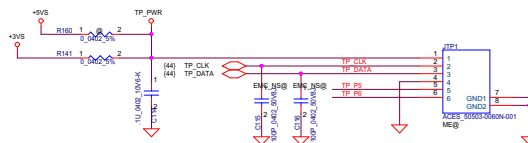
14"



15"

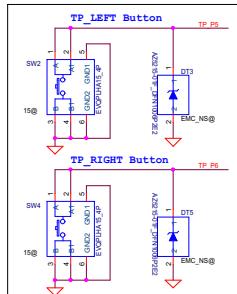
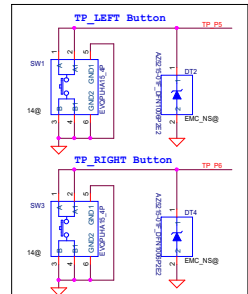


	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS15_14	KS13_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS01_15
KB_14	KS04_14	KS01_15
KB_15	KS07_14	KS01_15
KB_16	KS08_14	KS01_15
KB_17	KS06_14	KS01_15
KB_18	KS03_14	KS01_15
KB_19	KS01_14	KS01_15
KB_20	KS01_14	KS01_15
KB_21	KS01_14	KB_LED_FWR_15
KB_22	KS01_14	CAPS_LED#_15
KB_23	KS01_14	VDD_15
KB_24	KS01_14	NUM_LED#_15

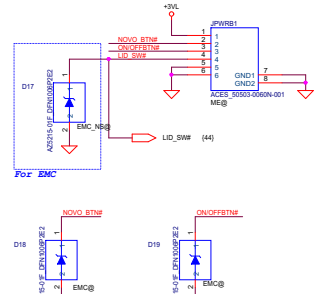


For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R

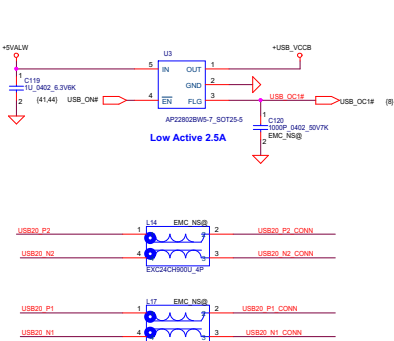
Change to same as ACLUA



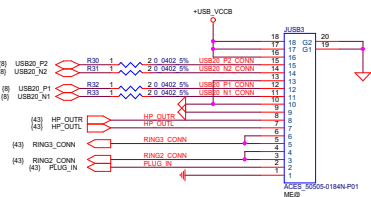
PWR/B Connector



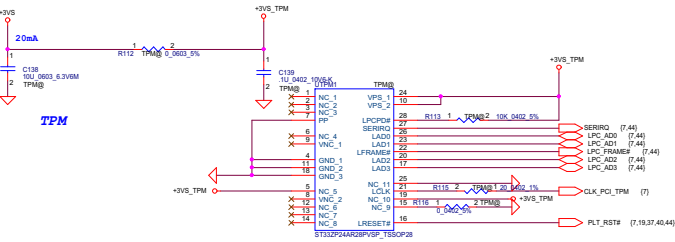
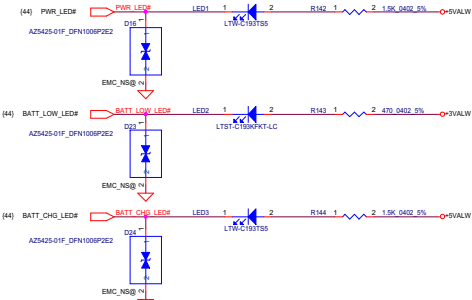
Right Side USB2.0 Port X 2 (USB/B)



USB I/O Connector

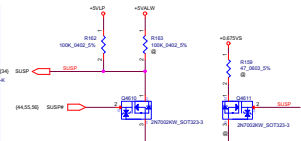
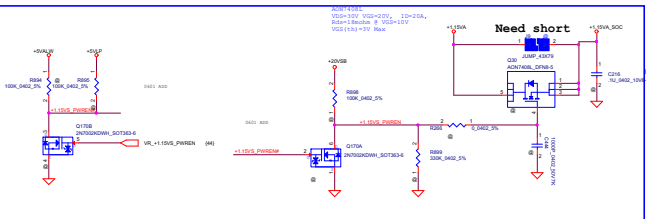
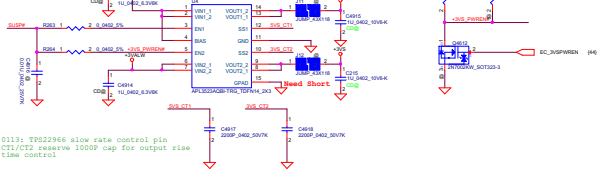


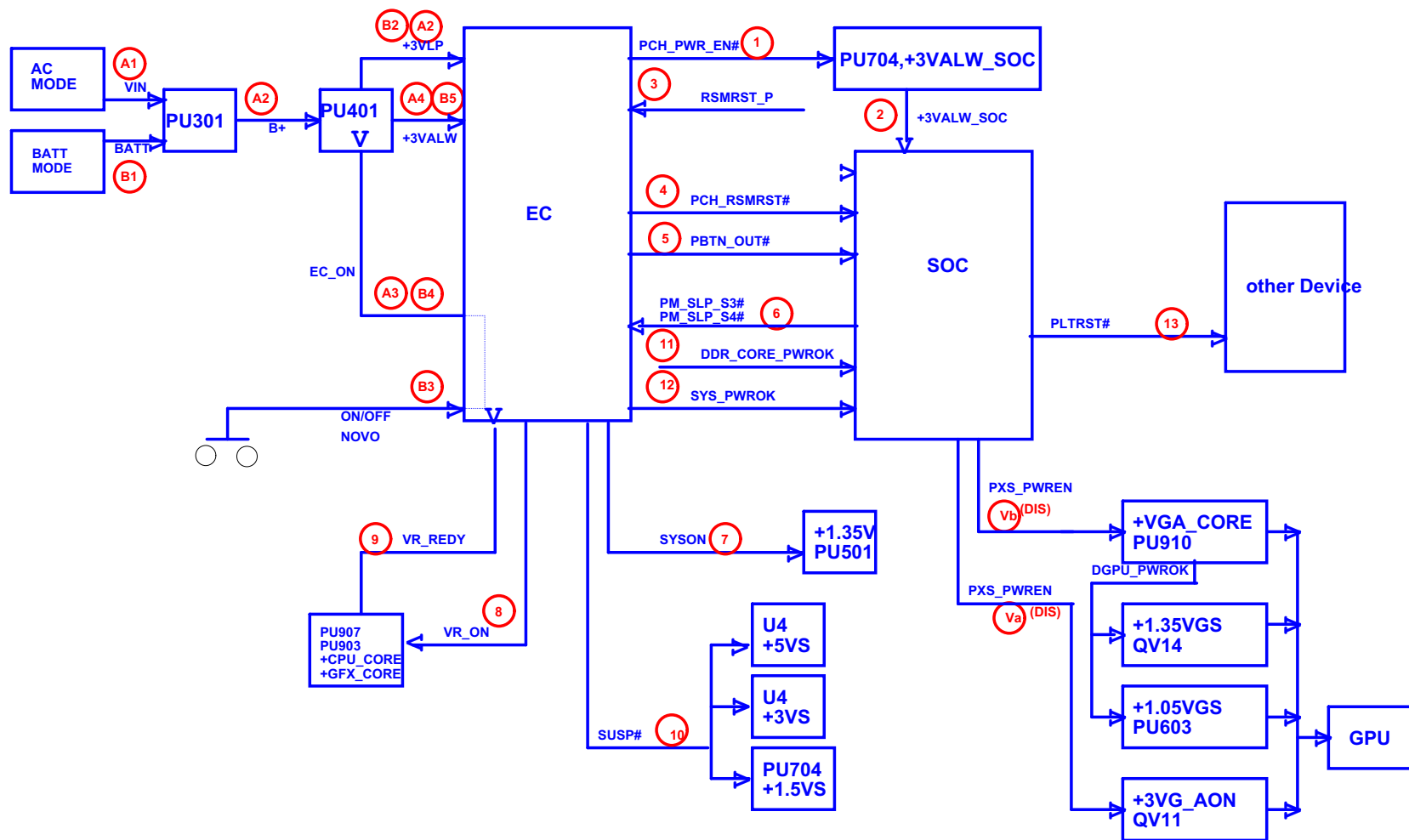
LED

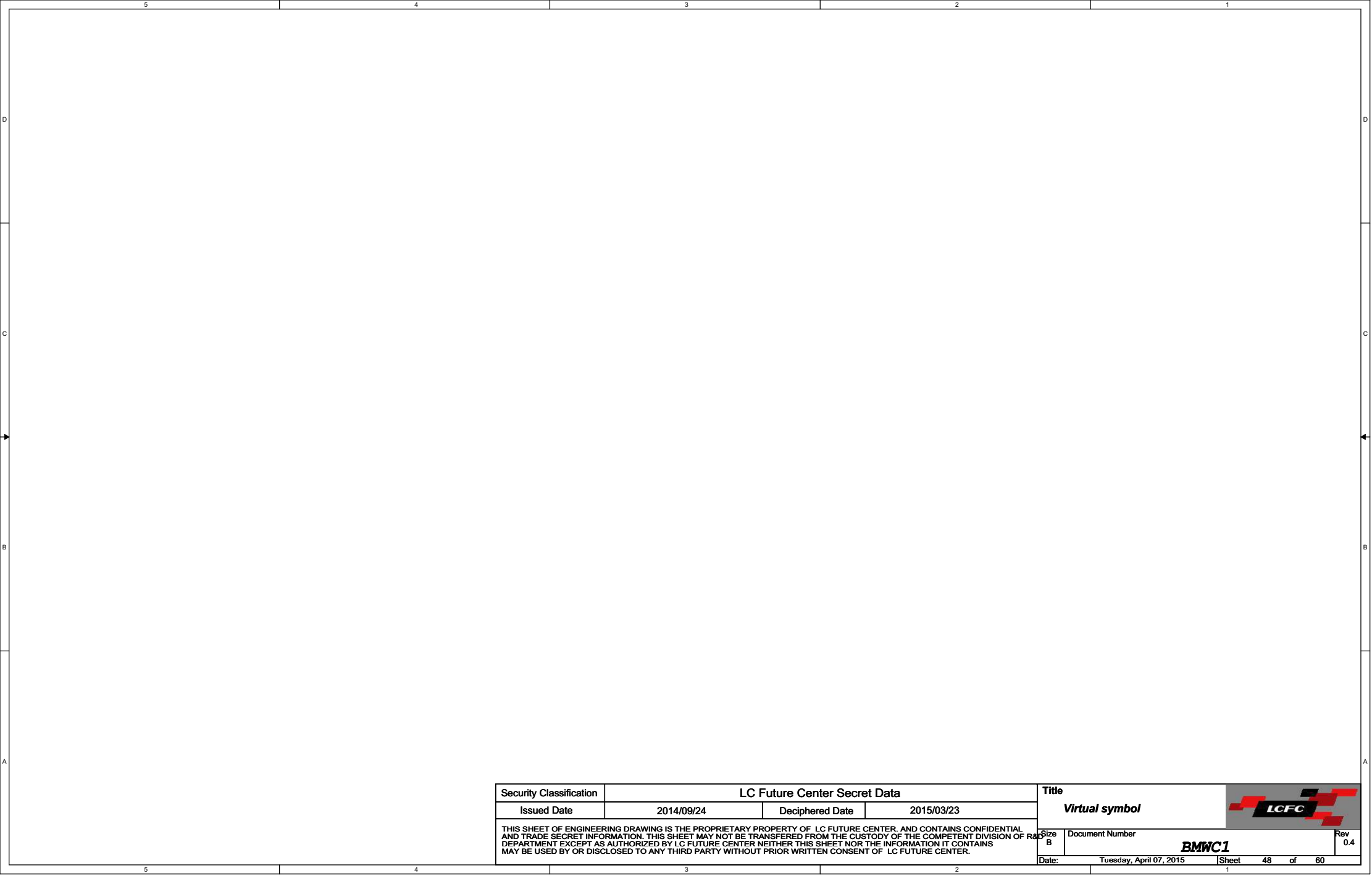


+5VALW to +5VS

+3VALW to +3VS

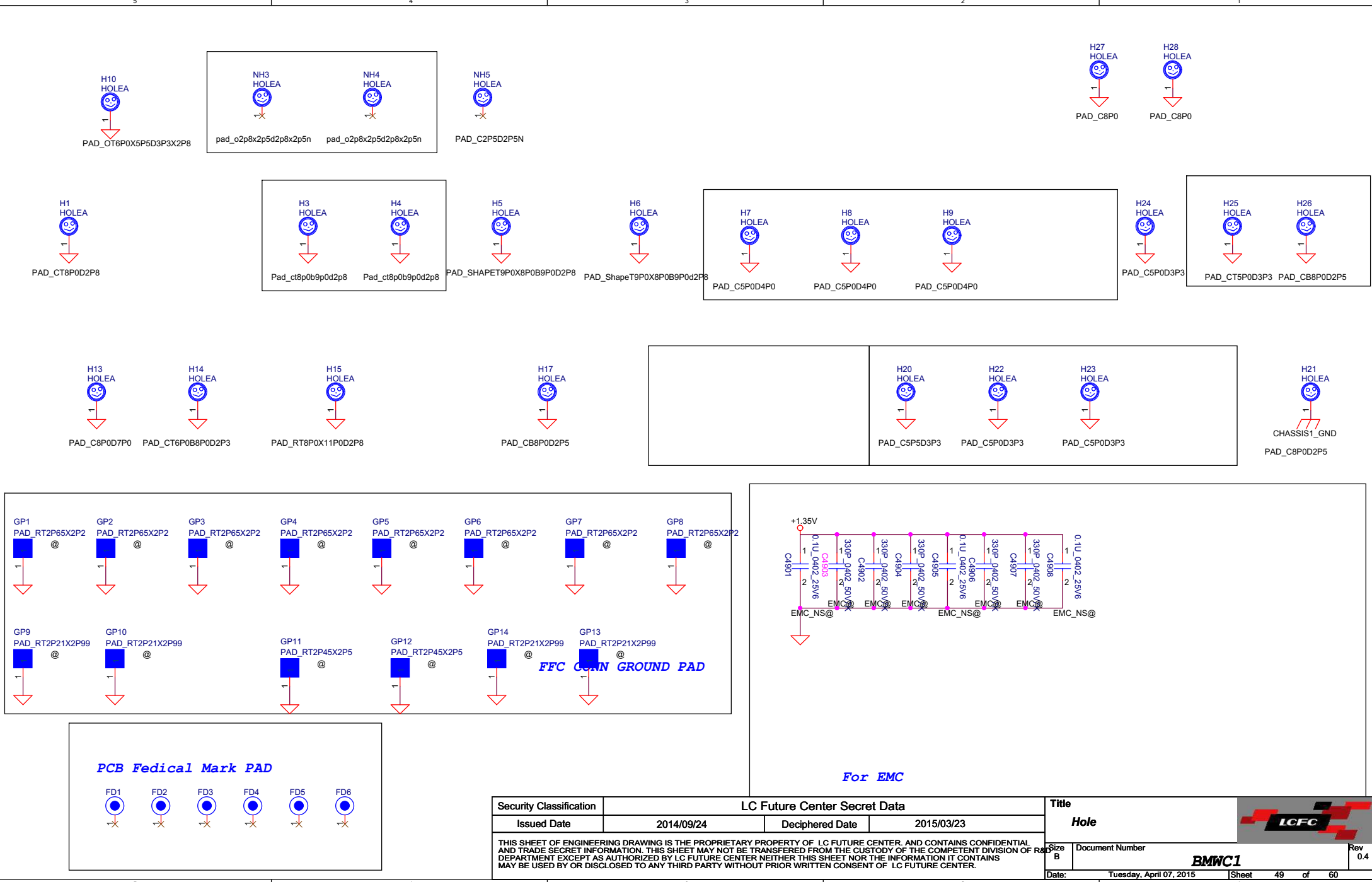




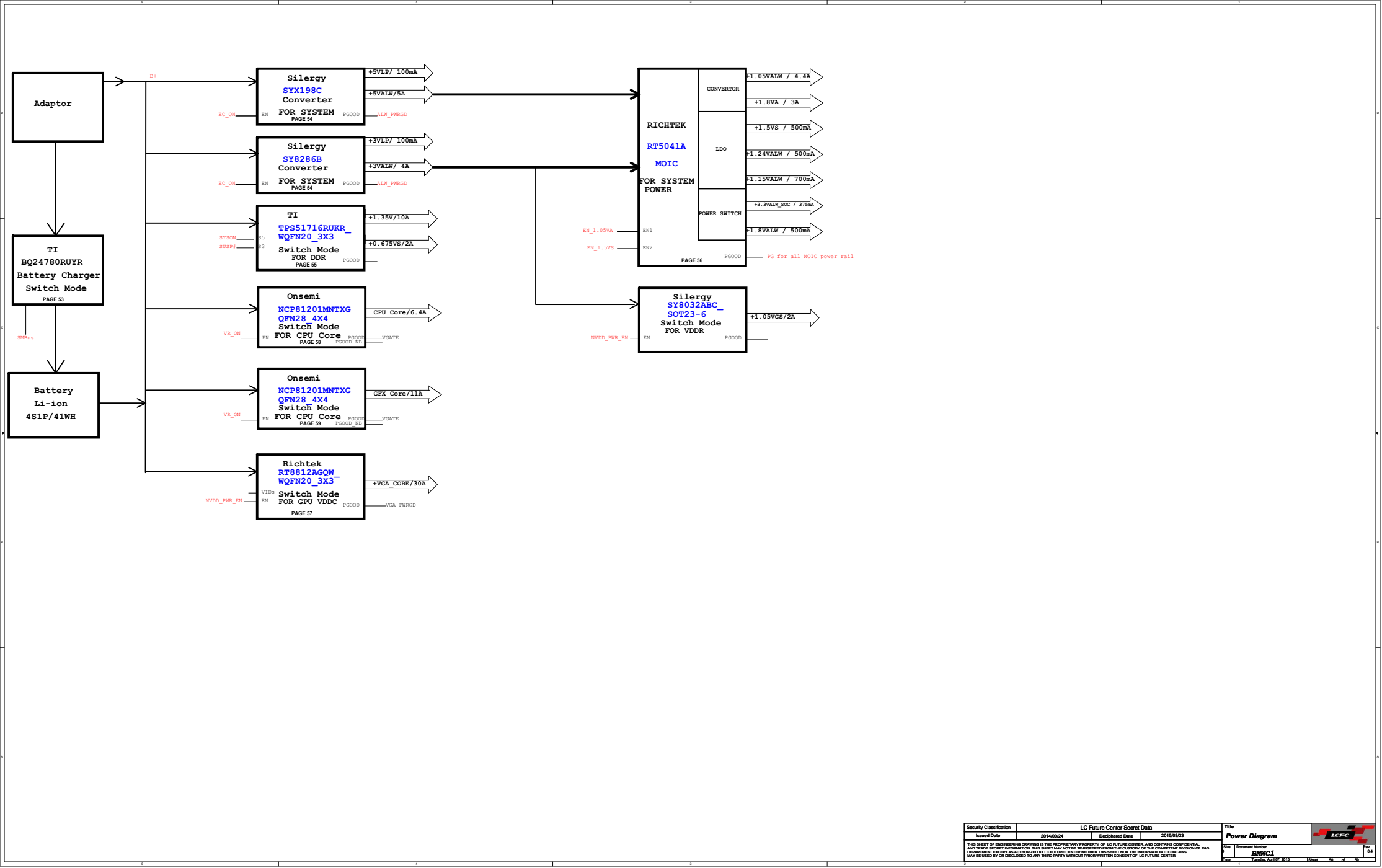


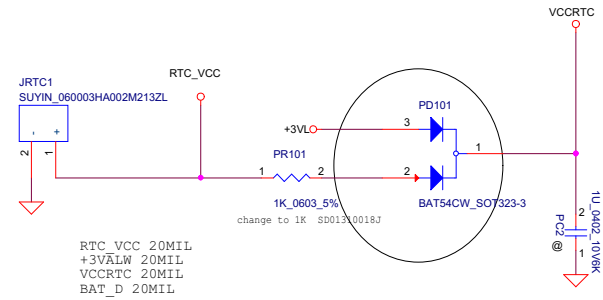
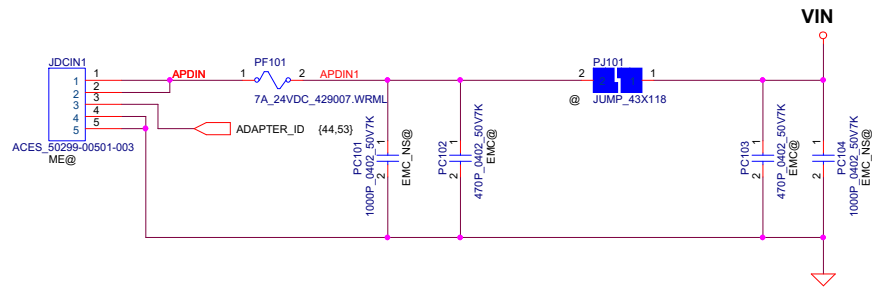
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Issued Date	2014/09/24	Deciphered Date	2015/03/23	Virtual symbol			
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				B			
				Date:	Tuesday, April 07, 2015	Sheet	48 of 60

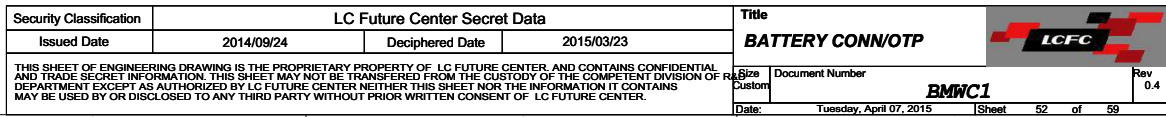
Rev 0.4

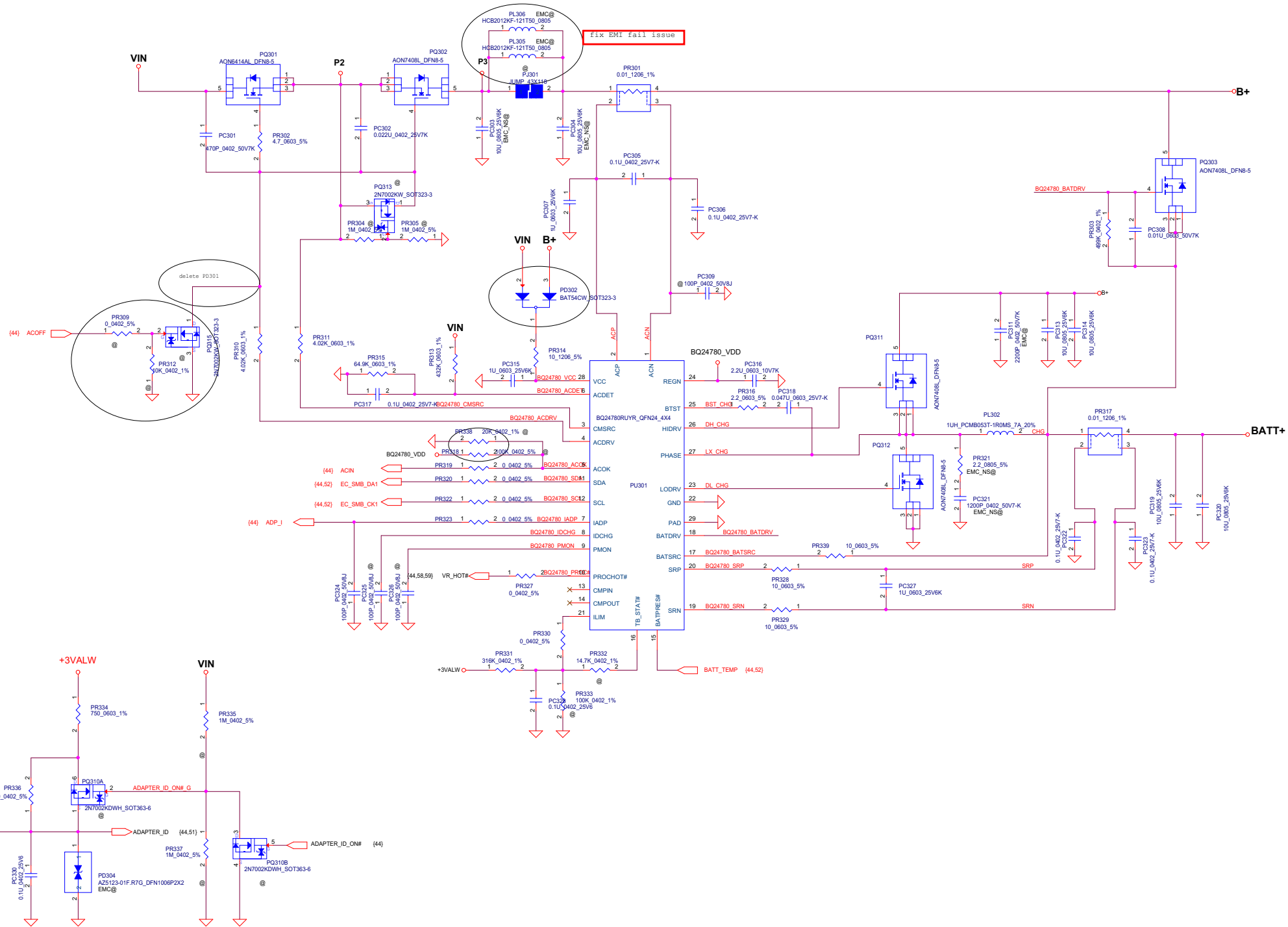


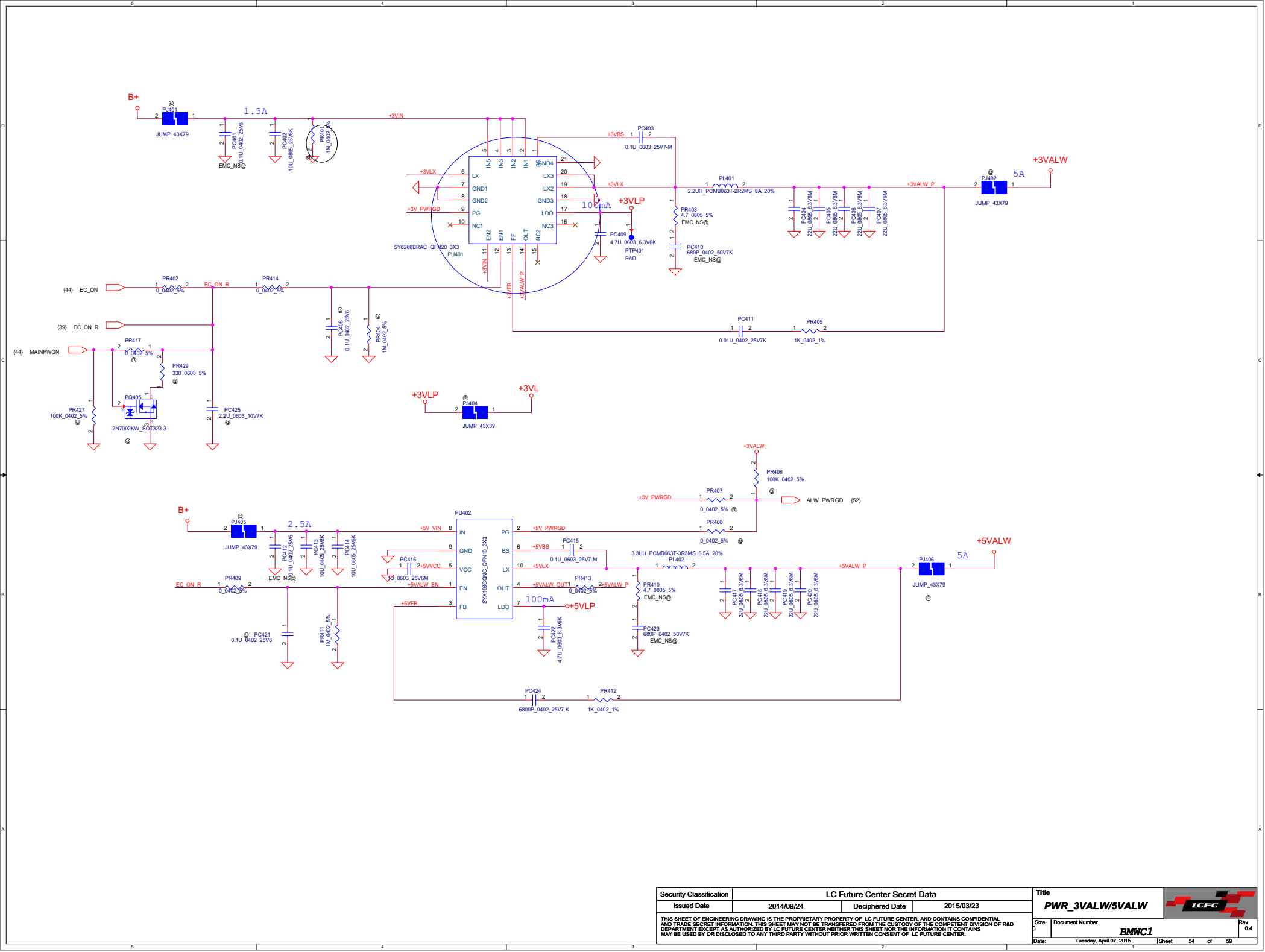
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Date:		Tuesday, April 07, 2015					Sheet 49 of 60		BMWC1		

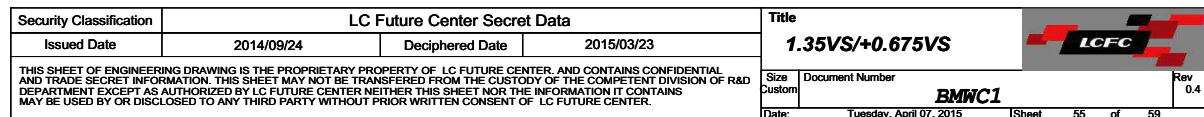













```
for CPU TDC from 6.4A change to 7.7A
PR785: 21K-24.3K/0402/1%
PR783: 7.68K-9.31K/0402/1%
PR778: 20.5K-19.6K/0402/1%
```

